BEAM

NetProcFpga System

Initial Proposal for networked FPGA Processing System

Project	NetProcFpga
Date	2019-07-19
Reference	NetProcFpgaProposal-1
Author	Dr Terry Barnaby

Table of Contents

1. References

- The existing Beam NetProcFpga system.
- The Dune Neutrino Experiment: https://www.dunescience.org/

2. Introduction

The Dune Neutrino Experiment will require data capture and processing systems to take the detector's sensor inputs via optical connections, process and store in a non volatile FIFO the incoming data streams and provide network access to the data streams and data. There will be in the order of 150 servers and 300 FPGA based real-time processing engines each with a large DDR RAM FIFO and 1 Terra Bytes of NVMe FLASH storage.

The plan is to use conventional PC based servers with two custom made PCIe FPGA processing boards installed in each.

For a previous client Beam has designed and produced a networked FPGA processing system. An updated version of this system could provide a better alternative to using standard servers with separate PCIe FPGA boards. The following is an initial proposal for such a system with information and pictures of our existing system.

3. Features

1. System based on tightly coupled SOC CPU with FPGA. Server, IO and FPGA processing all on one PCB.
2. Physically small 1U case format for reduced racking system volume.
3. Optical fibre inputs for one or more input data streams (optimise to FPGA processing capabilities).

4. 3 or 4 x 10 Gigabit Ethernet interfaces (Could implement 100 Gbits/s if needed).
5. Simple and low power single PCB units for reliability, lower power usage and lower cooling requirements.
6. Lower cost than separate servers with custom FPGA processing boards.
7. Using a separate CPU rather than using an FPGA core CPU allows a lower cost FPGA to be completely managed from the CPU and provides much higher performance CPU abilities along with IO hardware engines built into the SOC CPU.
8. Possibly use an IO front-end PCB module to allow usage of different connectors/frontend processing hardware for other uses.

4. Proposed NetProcFpga System

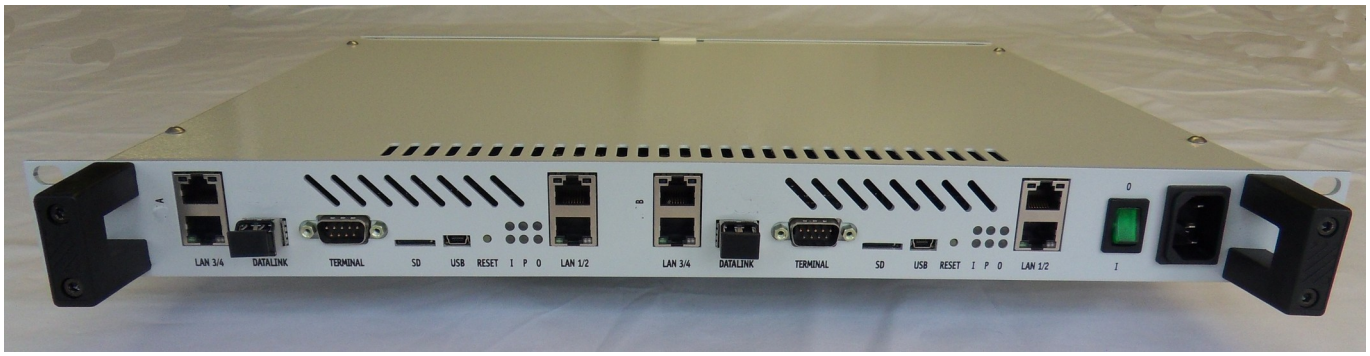


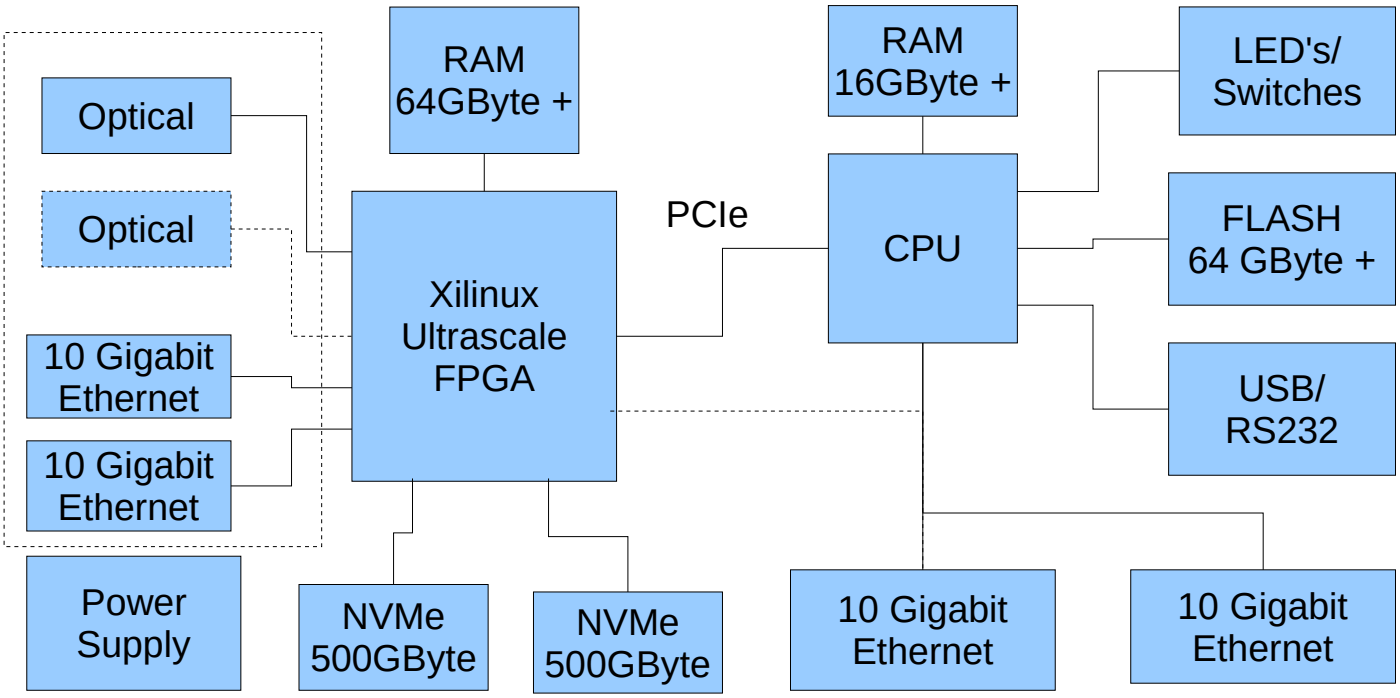
Figure 1: Current Beam NetProcFpga System

The proposed system would physically consist of a number of 1U rack mounted modules. Each 1U case would have a two custom Server/FPGA processing board's installed.

Figure 2: Current Beam NetProcFpga System Internals

Each NetProcFPGA board would have a Xilinx 7 series Ultrascale FPGA closely coupled with a power full SOC CPU running the Linux OS to provide control and data communications functionality and if needed some data processing abilities.

The systems block diagram would be as follows:



The system would probably be based on the latest Xilinx Ultrascale FPGA series with one of these devices installed. The exact type and size of the FPGA will be based on functional requirements and cost. A 64 bit embedded multi-core SOC CPU would be included to provide system control and communications. This could be based on a SOC ARM 64bit architecture with additional DSP processing engines or an x86 based chip. The board would have a single or dual optical interfaces connected directly to the main FPGA. Four 10 Gigabit Ethernet interfaces would provide communications with external systems two connected to the CPU and one connected to the FPGA. Both the FPGA and CPU would have there own DDR4 RAM which would be accessible from both the CPU and FPGA probably using plug in DIMM modules so size can be chosen.

The system would run Linux from the on-board flash and be fully self contained. The board power requirements would likely be a single 12V DC supply fitted inside the 1U case. Two of these boards would be designed to be installed in a simple 1U 19inch case with all external connectors and LED's on the front side edge of the board.

Some of the benefits of this system over a separate server based system would be:

- Simpler system. Less components needed for production and less prone to faults.
- Tightly coupled CPU/FPGA system for simpler and high performance operation.
- The system is simpler to maintain due to its single parts structure. Faults would be handled by one vendor.
- Physically smaller form factor 1U.
- Lower power usage and reduced cooling requirements. Probably about 60 Watts per board depending on processing requirements.
- Lower cost. The server and FPGA modules are all on one board sharing power supplies, cases etc.
- Could be used for other purposes. We would likely design the board with a FPGA front end PCB

module so different IO connectors and electronics interface hardware can be used for differing processing requirements.

- A full system based on this architecture, matching the 150 server and 300 FPGA modules plan, would likely be significantly cheaper overall (including development costs).

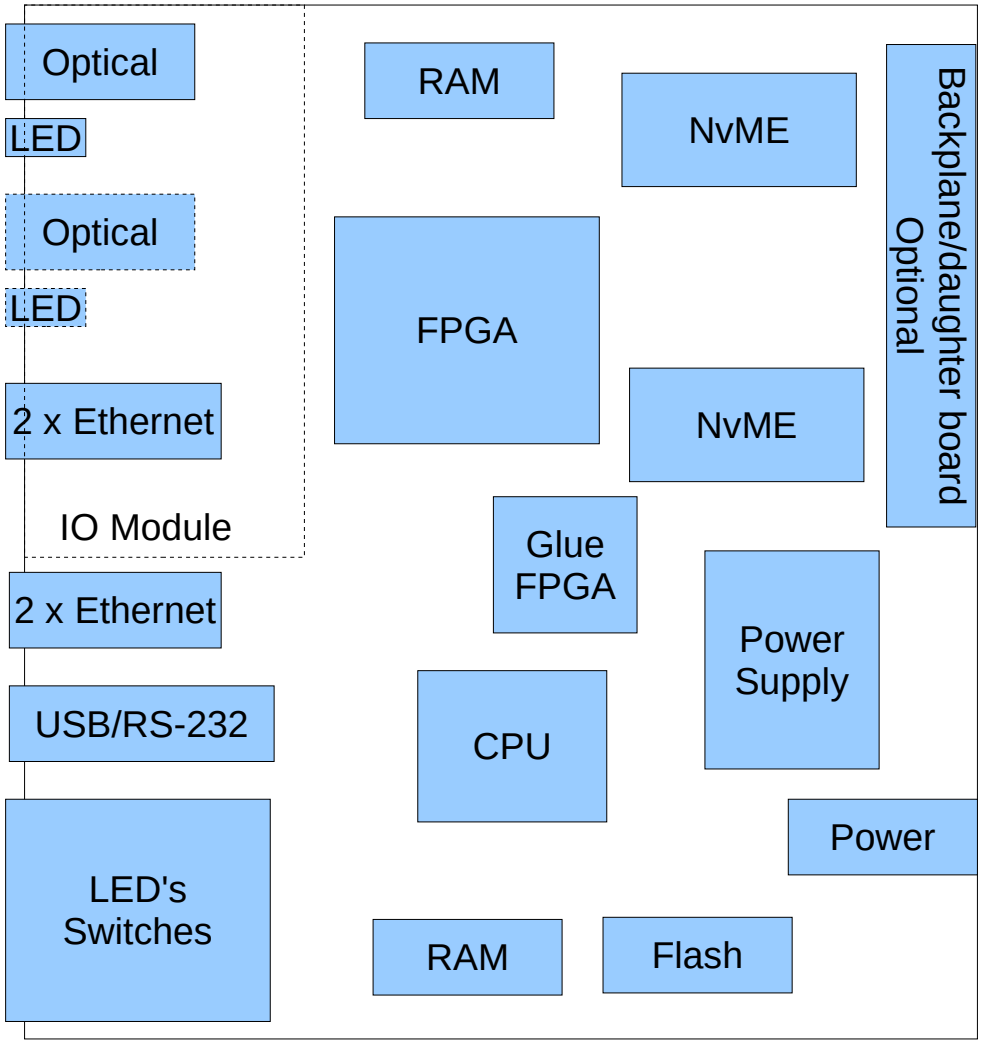
5. Design options

Some possible design options.

1. For the SOC CPU we could use a QorIQ LS 2040A SOC. This has four and eight ARM® Cortex®-A57 cores and can support up to 5 x 10 GBit Ethernet and PCIe. http://cache.freescale.com/files/64bit/doc/fact_sheet/LS2080AFS.pdf
2. Another option for the SOC CPU is the AMD Ryzen V1000 chip: https://www.amd.com/en/products/embedded-ryzen-v1000-series. This has 4 cores running at 3.6 GHz with a TDP of 12 – 25 Watts and a graphics processing engine that could be used for data processing.
3. There are other SOC CPUS with higher performance and IO capabilities available as well.

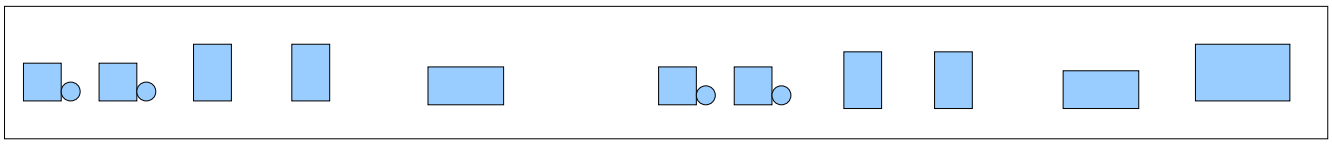
6. Board layout

A possible PCB layout is shown below.



7. Case

These show a possible front panel layout for the 1U case.



Front Panel layout with two cards

8. Work Required

We already have designed a version 1 NetProcFpga system that has been produced in numbers and is working 24/7 for our clients. The work needed to develop a version 2 board that would be updated with a more recent FPGA and higher performance SOC CPU, to better suit the Dune project would require the following design and development work:

- Overall system research and design (Component choice etc). This will carry out a detailed design evaluation. It will be carried out with The Dune project to ensure current and possible future requirements are met and lead to a detail specification of the system.
- Design NetProcFpga board hardware.
- Produce prototype boards. We will produce two or three sets of prototype boards leading to the production level boards.
- Produce prototype cased units. This will use our custom designed 19inch 1U cases
- Port Linux System to the system. This may be available for the SOC chosen but we would, at least, port our high performance PCIe FPGA device driver to the system and configure the system for the hardware present.
- Implement and provide documented FPGA interface IP for the FPGA and software libraries and examples to allow the Dune project to develop the FPGA and software for the system. We would provide a set of example software and firmware providing the boiler plate system level code needed for the project but without the detailed control and processing software/firmware needed.
- Test the system.
- We can take the unit through a CE approvals process including emissions and susceptibility testing if desired.
- Produce production system information. Information required to produce the boards.
- After acceptance, produce 150 of these systems (300 FPGA’s) for the Dune project.

9. Time scales and Costs

These costs are early ballpark estimates of the work involved and is based on the expected components involved. The system research and design phase may alter the choice of components used and hence the costs. In particular the Xilinx FPGA type and speed used will affect the board production cost significantly.

Estimate of System Design and Development	£165,000.00

3 sets of 3 Prototype cards	£33000.00
Optional CE testing	£11000.00
Early ballpark estimate of production unit cost (2 x server/fpga boards in 1U case). This highly depends on FPGA type used, RAM size, SOC CPU used and size of NVMe etc.	£9000.00 (150 required for 300 FPGA channels)

The expected project time scales are as follows:

From project start to first prototype systems	11 Months
From end of testing to first production boards	2 Months

Time scales depend on component availability and BEAM's work schedules during the projects life time.

Additional work and support can be carried out on a per day basis or by separate work contracts.

All prices exclude VAT and are valid for 3 months from the date of this estimate.