| Project | CERN-TMS |
|---|---|
| Date | 2006-11-17 |
| Reference | Cern-tms/systemDesign |
| Version | 1.0 |
| Author | Dr Terry Barnaby |

# Table of Contents

# 1.    References

● IT-3384/AB: Technical Specification for a new trajectory measurement system for the CERN Proton Synchrotron.

● Alpha Data's product data sheets.

● Emailed questions answered by Jeroen Belleman of CERN.

● Visit to CERN on 2006-06-20

Document:          cern-tms/systemDesign                                          Page 1 of 11
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- Various email conversations with Jeroen Belleman and Grzegorz Kasprowicz of CERN

- TMS design documents: pupeBoardDesign, pupeFpgaDesign and softwareDesign.

- CERN Visit: 2006-11-16

# 2. Introduction

This System Design document concerns the overall design of the new Trajectory Measurement System (TMS) for the CERN Proton Synchrotron. The system captures and processes the data from 120 analogue signal acquisition channels, organised into 40 separate Pick-Up channels. FPGA technology is used to implement the data capture and signal processing functionality in real-time. The system will be used to derive the positions of particle bunches undergoing acceleration and manipulation in the CERN Proton Synchrotron.

This System Design document gives an overview of the design to implement the CERN Trajectory Measurement System to match the technical specification as given in the "IT-3384/AB Technical Specification" document together with additional input from emails with CERN's staff.

There are separate design documents for each of the major component parts. These are: pupeBoardDesign, pupeFpgaDesign and softwareDesign.

# 3. Design Features

The main design features of the system include:

- High degree of modularity. The system is split into 3 + 1 independent processing modules. Within each processing module there can be 5 PU processing engines each processing 3 of CERN's PU's. Each of these PU processing engines (PUPE) has 9 analogue inputs, 1 digital clock input, 16 general purpose digital I/O ports and a large Xilinx Virtex-4 FPGA.

- High degree of board level component re-use allowing quick and easy swapping of faulty components.

- Large level of common of the shelf (COTS) components reducing system development costs, reducing project risk and easing maintenance.

- Based on the flexible, powerful and recent Xilinx Virtex-4 FX FPGA chips providing leading edge firmware configurable, high performance data processing.

- Spare FPGA capacity for additional algorithms.

- More memory than technical specification requires. The system will have at 256Mbytes of

Document:         cern-tms/systemDesign                                                      Page 2 of 11
Web:              www.alpha-data.com
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memory available per PU rather than the 128MBytes called for in the specification. This will allow a longer data sampling period to be performed or allow more data to be stored per cycle.

- Open-source software for flexibility and ease of customisation.

- Relatively low power and hence reduced heat dissipation and reliability.

- Housed in an industry standard compact PCI rack system for a robust, off the shelf, enclosure system.

# 4.   Overall System Design

The system hardware design has been based, as much as possible, on common of the shelf (COTS) components available from Alpha Data and other sources. There is one, board level, component that will be specially designed and manufactured for the system: the Pick Up processing Engine (PUPE). This compact PCI board is based around Alpha Data's **ADM-XRC/FX100-10/1G FPGA** PMC module's design. It has a Vertex-4 FX100 FPGA together with 9 analogue to digital converter's and digital timing/test signal interface circuitry. The system uses the industry standard compact PCI (cPCI) rack mounted bus system to house the main processing boards, power-supplies and provide fan cooling to the system's hardware. The system will have the following connections:

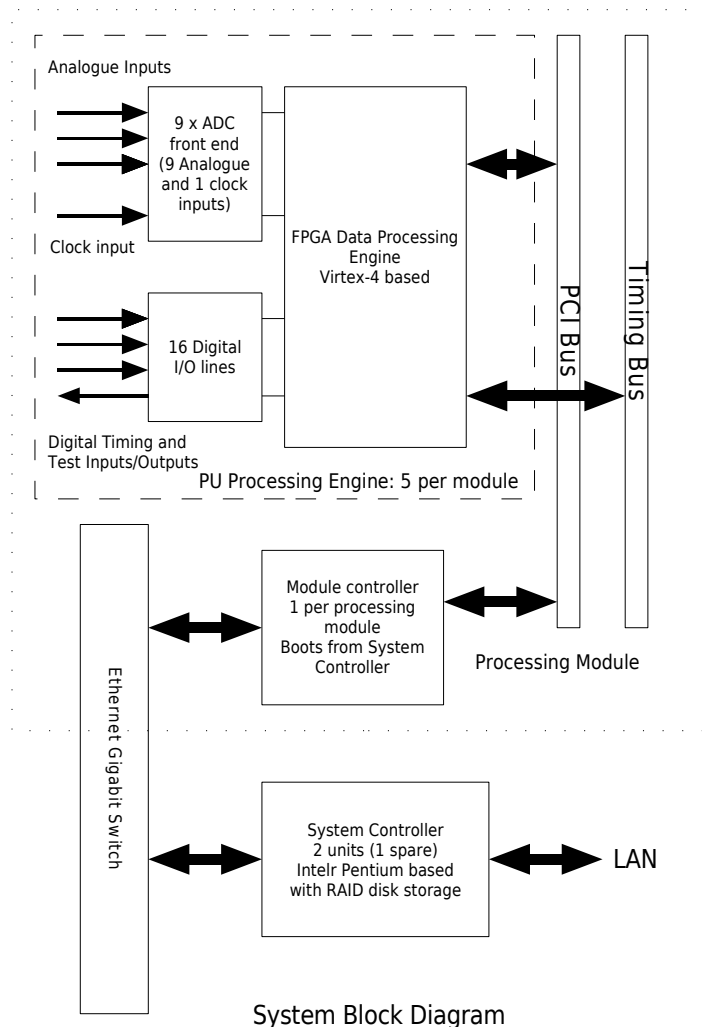| *Name* | *Number* | *Description* |
|---|---|---|
| ADC Input | 120 + 30 spare | Analogue signal inputs. 1 Volt peak to peak into 50 ohms. Sampled at 125 MS/sec at 14 bits. |
| 10 MHz system clock | 4 | Master system clock. The ADC's 125 Mhz sampling clock will be synchronised to this clock and all of the digital timing signals, except the Injection signal, will re-synchronised to this clock within each FPGA. Positive TTL into 50ohms. |
| FRef Input | 4 | Reference frequency. Positive TTL into 50ohms. (477KHz) |
| SCY Input | 4 | Start of a machine cycle. Positive TTL into 50ohms. (CYCLE_START) |
| CAL_START  Input | 4 | Start of calibration period. Positive TTL into 50ohms. (CAL_START) |
| CAL_STOP  Input | 4 | End of calibration period. Positive TTL into 50ohms. (CAL_STOP) |
| INJ  Input | 4 | Injection. Positive TTL into 50ohms.  (INJECTION) |

Document:          cern-tms/systemDesign                                                      Page 3 of 11
Web:                 www.alpha-data.com
Email:               terry.barnaby@beam.ltd.uk

| Name | Number | Description |
|---|---|---|
| H-CHANGE Input | 4 | Harmonic changes. Positive TTL into 50ohms.  (H-CHANGE) |
| ELFT  Input | 4 | End of Last Flat Top, effectively end of cycle. Positive TTL into 50ohms.  (CYCLE_STOP) |
| Spare Input | 4 | Spare digital inputs. Positive TTL into 50ohms. |
| Test outputs | 51 | Test signal outputs, one per PU. These will normal provide the synthesised FRef signal for test purposes but can be switched to provide certain other internal signals. 50Ohm Positive TTL outputs. |
| 1000/100/10 base T Ethernet | 2 | Network connections to CERN's systems for control and data access. RJ45 connectors. |

CERN will supply a set of 4 digital timing signals all, except for the injection signal, synchronised to the 10MHz master clock's positive edge. These signals will be connected to the digital timing inputs of each processing module where they will be distributed to each PU processing engine via a timing bus.

We have focused the system design on providing 24/7 service with minimal down-time in the event of a component failure. In order to achieve this and to ease system maintenance, system development time and testing the system has been designed in a modular way. The system consists of 3 identical processing modules and one reduced processing module as a spare. Each of these processing modules has its own power supply and an 8 slot cPCI backplane. The cPCI backplane has a PCI bus for board communications. Housed within each processing module is a conventional CPU based module controller and 4 or 5 PU processing engines. Each of the PU processing engines has 9 ADC's and 16 digital I/O lines connected to a Virtex-4 FX100 FPGA based processing engine. Thus each PU processing engine can acquire and process the data from 3 of the Proton Synchrotron's pick ups (PU's). This architecture was chosen to reduce system cost while providing FPGA processing from one of the latest Xilinx FPGA designs available.

The PU processing engines are interconnected with an 8 signal, 16 wire timing bus. The first PUPE in a processing modules has an extra panel containing connectors for the external timing signals. This first PUPE engine is configured to transmit these timing signals to all PUPE's in the processing module over the timing bus. The timing signal bus consists of an IDC ribbon cable connected along the front panels of the PUPE's. There is also the future option for passing the digital timing signals using the J3 connector of the cPCI backplane.

Document:          cern-tms/systemDesign                                                          Page 4 of 11
Web:               www.alpha-data.com
Email:             terry.barnaby@beam.ltd.uk

The processing modules are controlled from a master system controller through a local Gigabit Ethernet switch. The system controller is used for booting the individual processing engines and overall system control, data access and management. There are in fact two system controllers for system redundancy. Remote systems communicate with the system through the system controller, the individual processing modules are on a separate virtual or perhaps physical Ethernet based network.
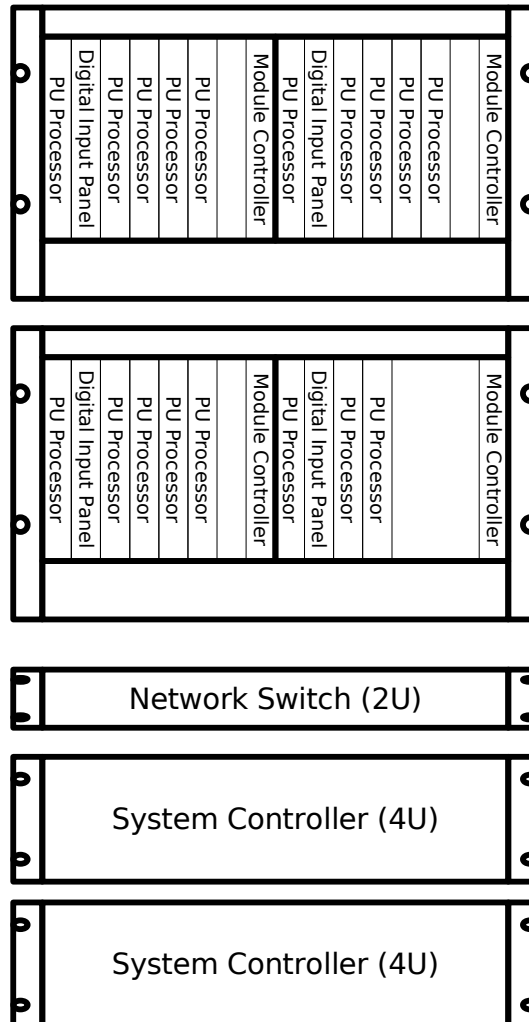


System Block Diagram

Document:        cern-tms/systemDesign                                    Page 5 of 11
Web:             www.alpha-data.com
Email:           terry.barnaby@beam.ltd.uk

# 5.  Physical Design

The system's physical design is based on the industry standard 19inch rack format. The systems 3+1 processing units are housed within two 9U cPCI backplane enclosures. Each cPCI enclosure houses two separate processing modules each managing 15 PU's. Each processing module has an independent power supply, set of fans for cooling and a module controller. The module controller is linked to the system controller using a Gigabit Ethernet interface.

Three of the processing modules implement the required 40 PU processors (actually 42). An additional processing module of 3 PU engines is spare, allowing either an individual PU processing engine to be replaced or a complete processing module to be replaced. The spare processing module could be left powered down for cold spares or powered up for hot spares. This spare processing engine could also possibly be used for testing new algorithms while the system is in use. There are spare cPCI backplane slots available in all of the processing modules for hot spares or additional processing or test modules.

Below the main processing modules is a Gigabit Ethernet switch that handles communications between the System Controller and the individual processing module controllers. If required two of these units could be supplied for redundancy or CERN's in house networking switches could be used.

There are two System Controllers for redundancy. Each of these controllers will have twin, long life SATA disks in a RAID configuration and run with identical software.

Document:        cern-tms/systemDesign                                    Page 6 of 11
Web:             www.alpha-data.com
Email:           terry.barnaby@beam.ltd.uk

Rack System

# 6. PU Processing Engine (PUPE)

The complete system has 17 PU processing engines each housed on a cPCI board. Fourteen PU processing engines are needed to support the 40 PU's and three boards are available as cold or hot spares. The PU processing engine consists of a custom cPCI board on which is mounted the Virtex-4 FX100 FPGA, ADCs and digital I/O interface components.

Document:          cern-tms/systemDesign                                        Page 7 of 11
Web:               www.alpha-data.com
Email:             terry.barnaby@beam.ltd.uk

The design makes full use of the Virtex-4 FPGA to provide a flexible hardware design solution that can be tailored in the FPGA firmware design.

Full details on the PUPE's design is contained within the pupeBoardDesign document.

The boards have been designed with built in Gigabit Ethernet interfaces. These provide the ability to use Gigabit Ethernet for all inter-board communications in future developments.

# 7.  FPGA Firmware

The FPGA firmware is the heart of the system. It implements the major real-time data capture and processing within the FPGA fabric.

Full details of the FPGA firmware design is in the pupeFpgaDesign document.

# 8.  Processing Module

Each processing module is independent of other processing modules. It consists of an 8 way cPCI backplane with power supply, a conventional CPU based module controller and 4 or 5 PU processing engines.

## 8.1.  Module Controller

The module controller will be a COTS component. It will have a conventional CPU, some boot FLASH memory, 1 Gigabyte of RAM, a cPCI bus interface and dual Gigabit Ethernet ports. The actual unit to be used will be the Concurrent Technologies PP 332/020  or the PP 410/03x. These boards are based on a low power Intel processors.

The module controller will boot from the main system controller over the Ethernet interface and will run a small Linux based operating system. It will be responsible for booting and managing the 5 PU processing engines (15 Proton Synchrotron PU's). Communications between the system controller and the individual PU processing engines will also be handled.

# 9.  System Controller

The system controller will be a standard Intel Pentium Xeon based computer system. It will be housed in a separate 4U 19" rack enclosure. The system controller will have 2 Gigabyte's of memory and dual SATA disk drives in a RAID configuration for disk redundancy. These disks will contain all of the TMS's software, FPGA firmware and configuration information. The system controller will have dual Gigabit Ethernet interfaces, one connected to the Gigabit switch that communicates with the processing

Document:          cern-tms/systemDesign                                         Page 8 of 11
Web:               www.alpha-data.com
Email:             terry.barnaby@beam.ltd.uk

module's controllers and one connected to the sites LAN for remote access to the system.

The system controller will not have a monitor, keyboard or mouse although these could be provided if required. All system configuration and maintenance will be carried out over the Ethernet network. The system will support the IPMI serial over LAN control interface for managing low level BIOS access if needed for complete software re-installation.

The system controller will run the Linux operating system.

Two identical system controllers will be provided for system redundancy. The second controller can be left powered down and then booted when required or left continuously running. Remote applications will be able to connect to either controller based on the IP address. Switching between the two system controllers would be handled by a configuration parameter.

As well as providing a control and data interface to the Trajectory Measurement System, the software on the system controller will implement system boot, system configuration, system test and fault diagnostics functions. This will be made available to operators via a web based interface as well as through a command line API.

# 10. Test Signal generator

As part of the design process we will produce a simple analogue test signal generator. This will be based on an 8 channel 150MSample/second arbitrary waveform generator PCI board. We will likely use the Chase DA8150-12-2M-PCI, http://www.chase2000.com/ board. A simple software application will be developed to drive this board with appropriate PS test signal patterns. We expect to drive the Sigma, DeltaX, DeltaY, SYSTEM_CLOCK, FREF, CYCLE_START, H-CHANGE and CYCLE_STOP signals with the signal generator.

# 11. System Software and API's

All of the system software will be based on the Linux operating system. This will provide a reliable an flexible system that can be easily maintained locally and remotely. All of the software will Open Source and thus all source code will be available. All of the system's special software will be available in source code form with an Open Source license.

All communications will be through the system controller which will support a simple, API to control and gather data from the system. The system controller will interrogate the individual PU processing engines via the local Gigabit Ethernet network and the module controllers. CERN can control and acquire data across the network interface from a remote system via the network based API or install their own programs on the system controller which will communicate with the system using the same API.

| Document: | cern-tms/systemDesign | Page 9 of 11 |
| Web: | www.alpha-data.com | |
| Email: | terry.barnaby@beam.ltd.uk | |

The system controller's API will accept "cycle control packets" from CERN's system describing each Proton Synchrotron's machine cycle. This information will allow the data captured to be tagged with the appropriate cycle information. This information will be sent to all of the PU processing engines along with configuration data such as the position of the PU engine within the Proton Synchrotron's ring.

Individual information tables will be distributed to each of the PU processing engines by this software using CERN's supplied data.

The system controller will be able to handle the swapping of hardware modules due to failure without any changes needed to CERN's control information.

The full design of the system software is given in the softwareDesign document.

The software will be developed on the GNU/Linux operating system and the Open Source GNU tool-set will be all that is required to develop the software.

# 12.  System Testing

As part of the development we will produce a test signal generator. This will produce simulated versions of the three PU signals and the main digital timing signals. The test signal generator will use an 8 channel arbitrary waveform generator PCI card. The card we will use is the Chase DA8150-12-2M-PCI, http://www.chase2000.com. This has 8 x 12 bit DAC channels at 150MHz with 1Megaword of memory per channel. This system will be used to simulate the real CERN Proton Synchrotron system. We will use CERN supplied, and other test signal data to drive the waveform generator.

The test signal generator will be used during the development of the hardware, FPGA firmware and host software of the system as well as for primary system testing. It will also be used during the maintenance and support phase so that we have a simulated CERN Proton Synchrotron system which will help with support.

After the initial support/maintenance phase, it will be possible to ship this test signal generator to CERN for system test, development and calibration purposes if required.

After the pre-series unit has been shipped to CERN, testing with real  the Proton Synchrotron system will be performed at CERN's site. This will be carried out with Alpha Data and CERN's technical engineers present.

# 13.  System Parts

This lists the high level system parts we have based our design on.

| | | |
|---|---|---|
| Document: | cern-tms/systemDesign | Page 10 of 11 |
| Web: | www.alpha-data.com | |
| Email: | terry.barnaby@beam.ltd.uk | |

| Qty | COTS | Part | Description |
|-----|------|------|-------------|
| 2 | yes | 6U backplane in 9U cPCI IEEE1101.10 compatible rack unit. PICMG2.0 Rev3.0 compliant with 400W power supply and 8 slots per unit. | This is the 8 + 8 slot 19inch 9U rack enclosure and power supplies for the processing modules. |
| 4 | yes | PP 332/020 or the PP 410/03x | A cPCI CPU controller board. 1GByte of RAM and GigaBit Ethernet interface. |
| 17 | no | PUPE Processing engine. Based on ADM-XRC/FX100-10/1G with 9 ADC's and Digital I/O on a cPCI board | These boards will be custom designed and manufactured. The FPGA design well be effectively the same as Alpha Data's ADM-XRC/FX100-10/1G FPGA module. |
| 1 | yes | Netgear GS116 | 16 port Gigabit Ethernet Switch. |
| 2 | yes | Supermicro server | System Controller. 19Inch rack mount 2U or 4U. Dual Xeon 1333Mhz FSB, 2GBytes of RAM, dual 250GByte SATA disks, dual Gigabit Ethernet, DVD drive. Two spare 64bit PCI slots, IPMI module. |
| 1 | yes | Chase DA8150-12-2M-PCI, http://www.chase2000.com/ | Arbitrary waveform generator PCI card |

# 14.  Internet Links for Components

Some Internet web links for the major component parts are given below:

| Item | Link |
|------|------|
| Alpha Data FPGA boards | http://www.alpha-data.com |
| LTC2255 ADC | http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1001,C1150,P11912 |
| Xilinx Vertex-4 FX100 | http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/index.htm |
| Compact PCI controller card | http://www.cct.co.uk/sheets/pp33202x.htm |

| | | |
|---|---|---|
| Document: | cern-tms/systemDesign | Page 11 of 11 |
| Web: | www.alpha-data.com | |
| Email: | terry.barnaby@beam.ltd.uk | |