CERN Project

Pickup Processing Engine

Design Specification

Revision 1.1.1

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1. Introduction

This Board Design Specification document describes the Pickup Processing Engine, subsequently referred to as PUPE, using FPGA technology and based on designs developed by Alpha Data in its range of PMC, PCI and PCI express products. The PUPE is designed as part of a Trajectory Measurement System for the CERN Proton Synchrotron. The overall processing system consists of 120 analogue signal acquisition channels, followed by digital signal processing to derive the positions of the particle bunches undergoing acceleration in the synchrotron. A PUPE card is capable of accepting 3 pickup input channels, each of which contains 3 analogue signals. Additional circuitry is provided to accept clock reference signals and interface with timing systems to synchronise acquisition across multiple cards.

A 6U panel assembly accompanies each group of 4 or 5 PUPEs to provide an interface for timing signals provided elsewhere in the Synchrotron and the master PUPE in a set.

2. Items Covered

The Alpha Data drawing references allocated to the following units covered in this specification are listed below.

AD01163 PUPE Board

AD01165 PUPE I/O Panel Assembly

3. Standards

The PUPE card is designed to meet PICMG CompactPCI® Core Specification 2.0 R3.0 and PICMG 2.16 R1.0 Packet Switching Specification.

The PUPE card is designed for RoHS-6 compliance.

The front panels for both the PUPE and PUPE I/O conform to IEEE1101.10 (EMC Panels).

4. PUPE Overview

The PUPE board design captures data from 3 analogue pickups and stores the data in memory for subsequent analysis. The acquisition of data is synchronised with other PUPE boards in the system using a timing bus and reference clocks provided by existing CERN equipment.

The PUPE board core processing sub-system is based on the Alpha Data ADM-XRC-4FX FPGA board which is a complete FPGA processing system with memory, IO and host interface resources.

The PUPE board operates in one of two modes depending on the position of the board within a rack. The first mode is called master and is used to receive system level timing information and output it to other PUPE cards in the rack. The second mode is slave and is used to receive timing information from a master PUPE.

The PUPE board provides additional outputs from the FPGA core that can be used for debug purposes.

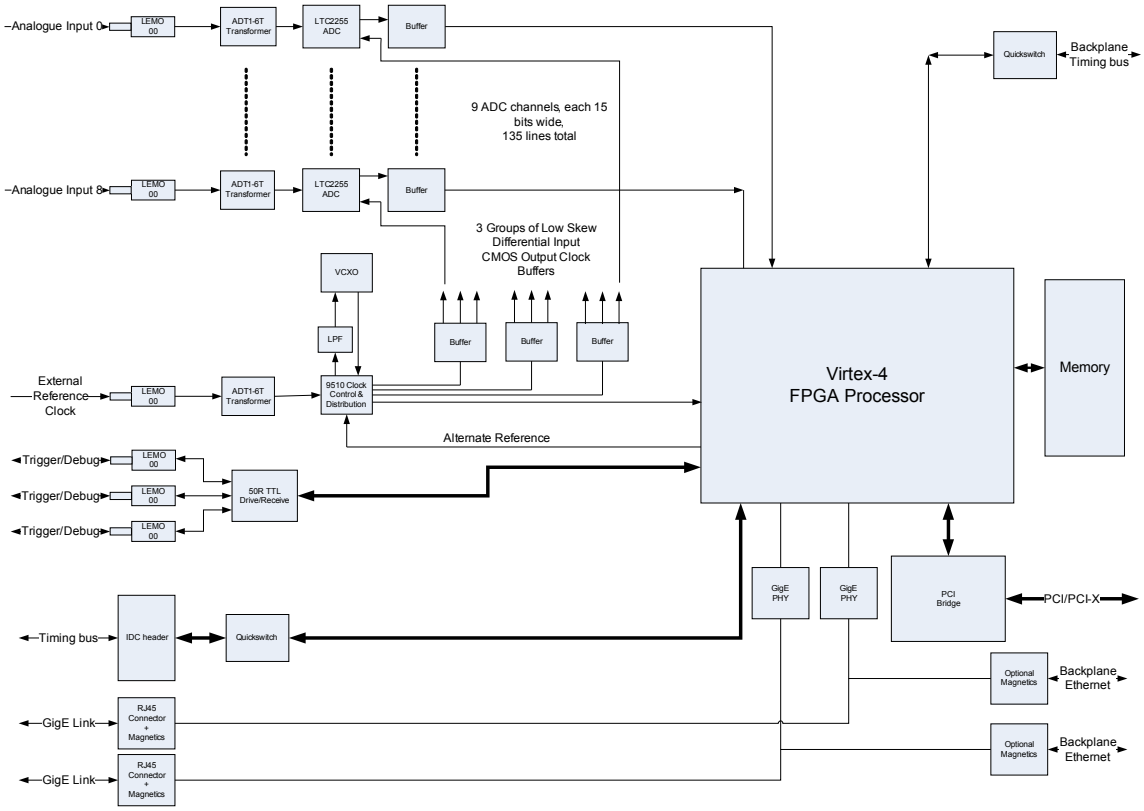

Figure 1 PUPE Board Block Diagram

Notes
1)Scale is 1:1 unless otherwise noted
2)Board width = 223mm
3)Board depth = 159mm
4)Length of front edge available for components =217mm
5)PCI connectors are 20 x45 and 132x45mm, 3 mm in from either edge
6)BGA version of VCX16374 available if required
7)SMA and LEMO 00 connectors fit in same footprint (10 mm min. between centres)

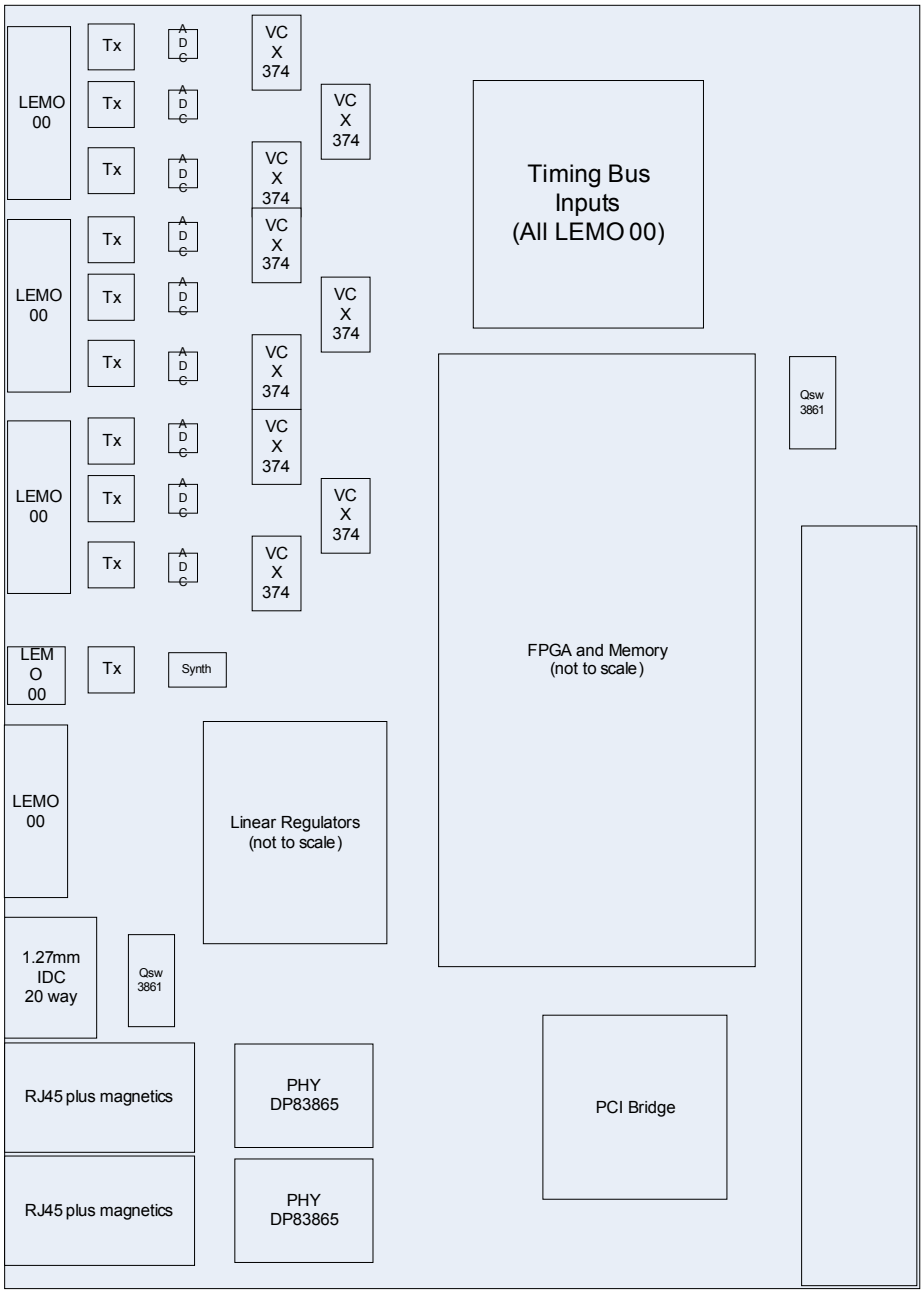

Figure 2 PUPE Board Layout

5. Analogue Capture

There are 9 analogue inputs on the PUPE card and they all sample synchronously using a common reference clock. Clock source selection and control over synthesis of the sampling clock is performed by the FPGA processor. The data captured from each channel is buffered and fed to the FPGA for further conditioning.

5.1. Interface

All analogue inputs, the 10MHz reference clock input, trigger/debug I/O and the inputs from the timing panel use LEMO 00 50Ω connectors.

5.2. Channel Performance

Each analogue channel has the following specification.

Converter	Linear Technology LTC2255
Maximum Sample Rate	125Ms/s
Input level	full scale +/- 1V, protected to +/- 4V
Input impedance	50Ω, transformer coupled
Input bandwidth	-3dB from 30kHz to 125MHz
Input filter	none
Coupling	transformer
ENOBS	>10.5
Input connector	LEMO

5.3. Clock System Performance

The clock input and distribution system on the PUPE has the following characteristics.

Input level	full scale +/- 1V, protected to +/- 4V
Input impedance	50Ω, transformer coupled
External frequency	10MHz
Sampling frequency	125MHz, synchronous to 10MHz, or asynchronous
Distribution Jitter	< 5ps RMS

5.4. Reference Clock

The PUPE normally requires a 10MHz reference clock in order to generate the 125MHz sampling clock for the converters.

The synthesis of the sampling clock is performed by an Analog Devices AD9510 which uses a VCXO to provide a stable low jitter reference running at 250MHz. This is then divided down by each of the output sections in the 9510 to produce four LVDS pairs at 125MHz each. Three of these are routed to

buffers feeding the clock inputs of the nine A to D converters and one is fed to the FPGA for reference.

The 9510 is a flexible device that can be used to produce other sampling clock frequencies if desired.

A low pass filter is driven by the 9510 and provides a control path for the VCXO. The characteristics of this filter are determined by passive components and can be customised for various PLL scenarios.

Programming of the 9510 is accomplished by a 4-wire interface controlled by the FPGA processor. This is necessary to set the PLL and output divider ratios and the selection of clock source.

The reference clock input can accept TTL level inputs and provides 50 Ohm routing and termination.

5.5. Alternate Reference Clock

An alternate clock source can be provided by the FPGA processor for debug and test purposes or for systems that do not provide or need a reference clock.

The FPGA Processor, which is an ADM-XRC-4FX PMC designed into the PUPE, incorporates a low jitter (around 1ps rms) programmable clock source, known as USERMGT clock, that is normally used to generate clocks for the Multi-Gigabit Transceivers in the Virtex-4 device but which can also be used within the fabric of the FPGA.

In the PUPE, this clock is also connected to the 9510 clock distribution device and can be used in systems where an external source is not available or where it is not necessary to synchronise to an external system.

An ICS843034-01 Femtoclock frequency synthesiser implements the alternate clock source to provide USERMGT clock and by default has two crystals of 25.0MHz and 26.5625MHz installed. The selection of the clock frequency to be generated by the Femtoclock is controlled by the PCI bridge in the FPGA processor and is fully supported by the ADM-XRC-4 Linux driver.

5.6. Sampling Clock Distribution

The 9510 produces 3 identical 125MHz sampling clocks using LVDS signalling. Each of these is routed to an Analog Devices AD9513 1:3 LVDS to LVDS/CMOS buffer to create 3 copies of the clock to service each cluster of A to D converters.

All differential traces are matched to control the skew between the groups of 3 A to D converters. The selection of LVDS outputs on the 9510 provides the ability to move two of the three clocks to allow fine deskew if required.

Internal to the FPGA Processor, a copy of the sampling clock is available to drive the PUPE data processing engine thus making the entire system synchronous. This clock is also used to capture the buffered data from each of the nine A to D converters.

5.7. Mode Control

Each converter has a MODE pin set to 1 of 4 values by jumpers depending on the output format required and selection of duty cycle correction. This function is not under control of the FPGA.

6. Timing Bus

The timing bus is a set of signals sourced from other CERN equipment that is used to synchronise activities in the PUPE card with all other PUPE cards in the system. The timing bus is received by a master PUPE card via a timing input panel and distributed to 3 or 4 slave cards in the same rack using either front panel or backplane interconnect.

The timing bus can accommodate up to 10 signals. The firmware loaded into the FPGA determines how these timing signals are interpreted.

All of the timing signals are synchronised to 125MHz by the master PUPE and output onto the timing bus for all slaves (and the master) to read. The FPGA processor will ensure that sufficient setup and hold time is available.

6.1. Master Mode Inputs

The master mode timing inputs are received via PCB mounted vertically orientated LEMO 00 connectors from the PUPE I/O panel.

The inputs are protected using quick-switches to allow 5V signalling at the connector whilst limiting the actual FPGA pin voltage to 3.3V.

All inputs are routed and terminated with 50Ω impedance.

6.2. Master/Slave Timing Interface

The master/slave timing interface permits a PUPE card to send or receive timing signals on a front panel connector to or from adjacent cards in the rack using a ribbon cable based bus. The signals are connected directly to the FPGA through a quick-switch for protection.

All of the signals on the bus are single ended and terminated in the characteristic impedance of the cable.

The last slave card in the rack implements the termination although all cards have the option to do so.

All of the timing signals are 3.3V LVTTL compatible.

6.3. Optional J3 Master/Slave Timing Interface

A similar set of timing signals are available for output on J3 and may be used in addition to or instead of those on the front panel.

7. Gigabit Ethernet Option

The PUPE card can optionally be fitted with physical layer components to support two 10/100/1000 Ethernet ports where the FPGA Processor is used as the MAC/CPU. These ports can be routed to the front panel or to the backplane via J3 in compliance with PICMG 2.16.

8. CPCI Pin Assignment Detail

The PUPE card supports J1, J2 and J3 as per PICMG specifications. It does not implement hot-swap capability and is compliant only with 3.3V PCI signalling systems.

8.1. J1 Pin-out

J1 conforms to PICMG 2.0 R3.0.

8.2. J2 Pin-out

J2 conforms to PICMG 2.0 R3.0.

8.3. J3 Pin-out

J3 is provided to support PICMG 2.16 packet based switching using IEEE802.3-2000 1000BASE-T. It also serves as an alternate interface for the PUPE rack timing bus.

The pin assignment of J3 uses sparse population of signals. The timing bus signals, T1- to T8-, are located to avoid becoming aggressors to the differential signals of the two link ports. The link ports use spare BP(I/O) signals on rows 14 and 19 connected to ground for additional isolation.

19	GND	GND	GND	GND	GND	GND	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	GND	GND	GND	GND	GND	GND	GND
13	GND	NC	NC	NC	NC	NC	GND
12	GND						GND
11	(2)						(2)
10	(2)						(2)
9	(2)						(2)
8	GND						GND
7	GND						GND
6	GND	T1+	T2+		T3+	T4+	GND
5	GND						GND
4	GND	T5+	T6+		T7+	T8+	GND
3	GND						GND

2	GND	T9+	T10+				GND
1	GND	(1,16)	(1,16)	(1,16)	(1,16)	(1,16)	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 1 CPCI J3 Pin Assignments

Notes.

1,16 Refer to PICMG 2.16 R1.0.

9. Front Panel Timing Bus Pinout

The connector used on the front panel is a Molex part, number 87833-2019 which mates with the Molex 87568 series IDC receptacle.

The pin-out of the connector is shown below.

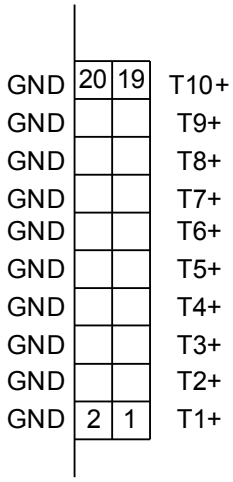

Figure 3 Front Panel Timing Bus

10. FPGA Processor

Refer to the ADM-XRC-4FX user manual for information in conjunction with this modified I/O section.

10.1. FPGA I/O Budget

The ADM-XRC-4FX is used as the basis for the FPGA processor and the I/O normally connected to the PMC Pn4 I/O connector and the XRM front panel adapter are reused in the PUPE for interfacing to the analogue subsystem and the timing bus(s). All other pin assignments used on the standard ADM-XRC-4FX card remain for compatibility with existing IP.

The budget available in terms of FPGA I/O pins is 146+64 = 210 pins.

10.1.1. Analogue Control (136 pins)

Each converter supplies 14 data lines to the FPGA and receives 1 clock for a total of 15 pins per channel and 135 in total.

In addition, the FPGA supplies 1 control line to all converters (tied to the OE and SHDN pins) to allow for global on/off.

10.1.2. Timing Bus (30 pins)

The timing system consists of three parts; master timing input, front panel timing bus and backplane timing bus.

The master timing input uses 10 pins on the FPGA to receive system wide timing information via the PUPE I/O Panel.

The front panel timing bus is a bidirectional interface shared between PUPE cards using 10 FPGA pins on a 20 pin header to output data from a master card and input data on a slave card.

The backplane timing bus is also a bidirectional interface shared between PUPE cards and uses 10 FPGA pins connected to J3 of CPCI interface.

10.1.3. Debug I/O (3 pins)

There are 3 FPGA pins dedicated to input or output of debug signals directly from the FPGA.

10.1.4. GigE Ports (30 pins)

There are two PHYs on the PUPE that can optionally be populated to support 10/100/1000 Ethernet. DP83865 MacPhyters are use for the physical layer and the MAC is provided in the Virtex-4FX device as a hard macro.

Each PHY uses the RGMII interface for reduced pin count using 4 bit DDR paths for a total of 12 pins plus the management interface of 3 pins giving 15 in total.

11. PUPE I/O Panel Assembly

The PUPE I/O Panel is compliant with IEEE1101.10 and serves the purpose of interfacing external CERN provided timing signals to a master PUPE card. The master PUPE card in turn distributes the timing signals to up to 4 other PUPEs within the rack.

The PUPE I/O panel allow connections to be made easily rather than directly onto the PUPE card itself which may cause mechanical stress.

The function of each of the timing signals on the panel is determined by the functionality implemented by the FPGA processor based on system requirements.

The layout of the 6U panel is shown below.

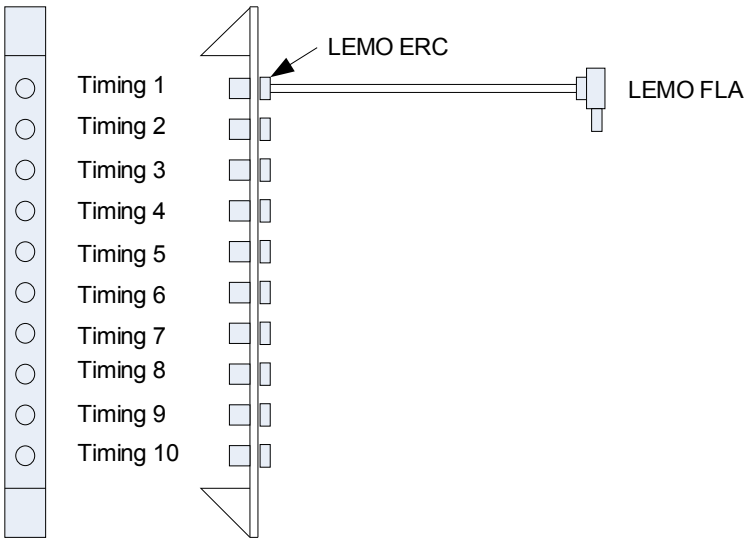

Figure 4 PUPE I/O Panel Outline

12. Revision History

Date	Revision	Nature of Change
05-11-2006	1.0	Created
12-12-2006	1.1	Updated with clock circuit revision