Preliminary System Design and Project Information

Project	CERN-TMS
Date	2006-06-23
Reference	Cern-tms/pre-design-1.5
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1. References

- IT-3384/AB: Technical Specification for a new trajectory measurement system for the CERN Proton Synchrotron.
- Alpha Data's product data sheets.
- Emailed questions answered by Jeroen Belleman of CERN.
- Visit to CERN on 2006-06-20

2. Introduction

This Preliminary System Design and Project Information document concerns the design, construction, commissioning, initial support and maintenance of a new trajectory measurement system for the CERN Proton Synchrotron. The system consists of 120 analogue signal acquisition channels, followed by digital signal processing to derive the positions of the particle bunches undergoing acceleration in the CERN synchrotron.

The Preliminary System Design document gives an overview of a design to implement the CERN Trajectory Measurement System to match the technical specification as given in the "IT-3384/AB Technical Specification" document. A detailed design will be developed in the first 2 months of the contract.

3. Design Features

The main design features of the system include:

- High degree of modularity. The system is split into 3 + 1 independent processing modules. Within each processing module there can be 5 PU processing engines each processing 3 of CERN's PU's. Each of these PU processing engines has 9 analogue inputs, 1 digital clock input, 16 general purpose digital I/O ports and a large Xilinx Virtex-4 FPGA.
- High degree of board level component re-use allowing quick and easy swapping of faulty components.
- Large level of common of the shelf (COTS) components reducing system development costs, reducing project risk and easing maintenance.
- Based on the flexible, powerful and recent Xilinx Virtex-4 FPGA chips providing leading edge firmware configurable, high performance data processing.
- Spare FPGA capacity for additional algorithms.
- More memory than technical specification requires. The system will have at least 256Mbytes of memory available per PU rather than the 128MBytes called for in the specification. This will

allow a longer data sampling period to be performed or allow more data to be stored per cycle.

- Open-source software for flexibility and ease of customisation.
- Relatively low power and hence reduced heat dissipation and reliability.
- Housed in an industry standard compact PCI rack system for a robust, off the shelf, enclosure system.

4. Overall System Design

The system hardware design has been based, as much as possible, on common of the shelf (COTS) components available from Alpha Data and other sources. There is one, board level, component that will be specially designed and manufactured for the system: the I/O interface board consisting of the analogue to digital converter front end and the digital timing/test signal interface circuitary. The system uses the industry standard compact PCI (cPCI) rack mounted bus system to house the main processing boards, power-supplies and provide fan cooling to the system's hardware. The system will have the following connections:

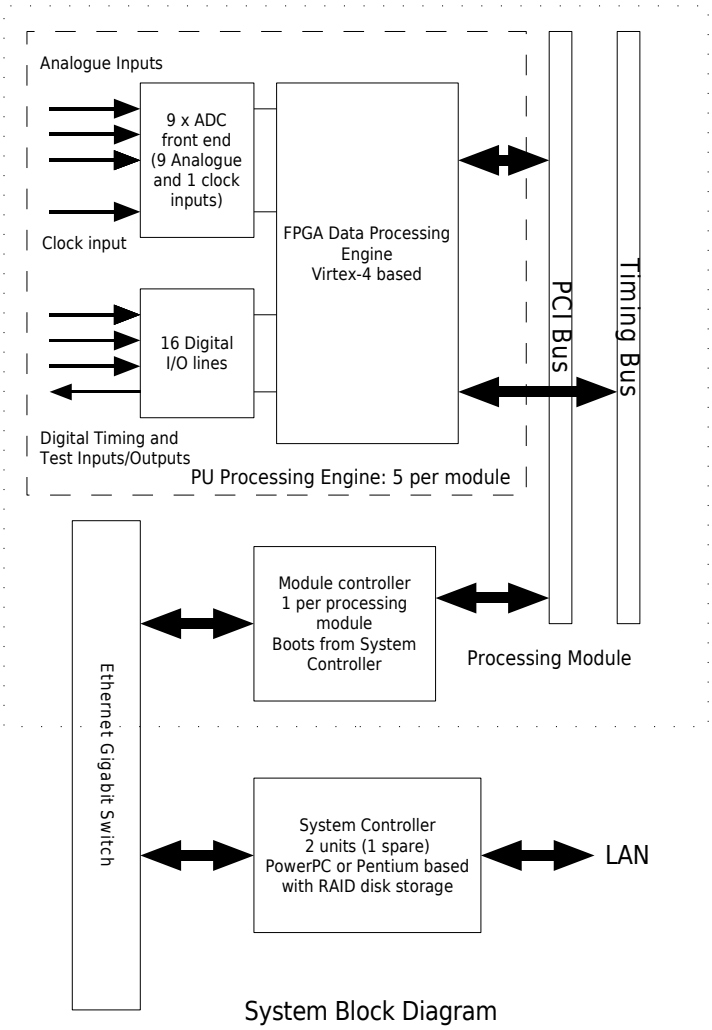
Name	*Number*	*Description*
ADC Input	120 + 30 spare	Analogue signal inputs. 1 Volt peak to peak into 50 ohms. Sampled at 125 MS/sec at 14 bits.
10 MHz system clock	4	Master system clock. The ADC's 125 Mhz sampling clock will be synchronised to this clock and all of the digital timing signals, except the Injection signal, will re-synchronised to this clock within each FPGA
Fref Input	4	Reference frequency
SCY Input	4	Start of a machine cycle
CAL_START Input	4	Start of calibration period
CAL_STOP Input	4	End of calibration period
INJ Input	4	Injection
H-CHANGE Input	4	Harmonic changes
ELFT Input	4	End of Last Flat Top, effectively end of cycle
Spare Input	4	Spare digital inputs
Test outputs	51	Test signal outputs, one per PU. These will probably carry the synthesised Fref signal for test purposes.
1000/100/10 base T	2	Network connections to CERN's systems for control and data

Name	*Number*	*Description*
Ethernet		access.

CERN will supply a set of 4 digital timing signals all, except for the injection signal, synchronised to the 10MHz master clock. These signals will be connected to the digital timing inputs of each processing module where they will be distributed to each PU processing engine via a timing bus.

We have focused the system design on providing 24/7 service with minimal down-time in the event of a component failure. In order to achieve this and to ease system maintenance, system development time and testing the system has been designed in a modular way. The system consists of 3 identical processing modules and one reduced processing module as a spare. Each of these processing modules has its own power supply and an 8 slot cPCI backplane. The cPCI backplane has a PCI bus for board communications and a separate bus for timing and test signals. Housed within each processing module is a conventional CPU based module controller and 4 or 5 PU processing engines. Each of the PU processing engines has 9 ADC's and 16 digital I/O lines connected to a COTS PMC FPGA processing engine module. Thus each PU processing engine can acquire and process the data from 3 of the Proton Synchrotron's pick ups (PU's). This architecture was chosen to reduce system cost while providing FPGA processing from one of the latest Xilinx FPGA designs available.

The processing modules are controlled from a master system controller through a local Gigabit Ethernet switch. The system controller is used for booting the individual processing engines and overall system control and management. There are in fact two system controllers for system redundancy. Remote systems communicate with the system through the system controller, the individual processing modules are on a separate virtual or perhaps physical Ethernet based network.



System Block Diagram

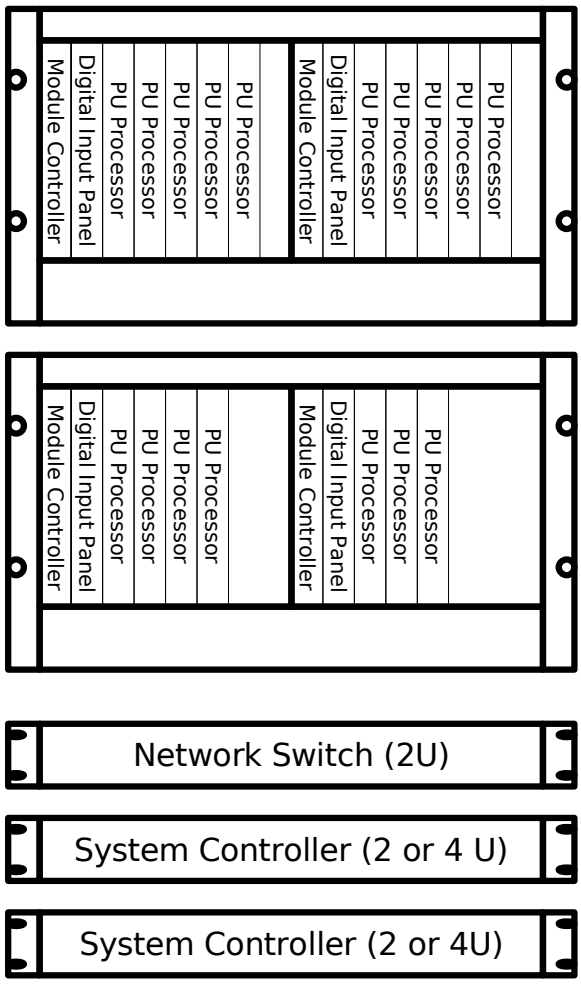
5. Physical Design

The system's physical design is based on the industry standard 19inch rack format. The systems 3+1 processing units are housed within two 9U cPCI backplane enclosures. Each cPCI enclosure houses two separate processing modules each managing 15 PU's. Each processing module has an independent power supply, set of fans for cooling and a module controller. The module controller is linked to the system controller using a Gigabit Ethernet interface.

Three of the processing modules implement the required 40 PU processors (actually 42). An additional processing module of 3 PU engines is spare, allowing either an individual PU processing engine to be replaced or a complete processing module to be replaced. The spare processing module could be left powered down for cold spares or powered up for hot spares. This spare processing engine could also possibly be used for testing new algorithms while the system is in use. There are spare cPCI backplane slots available in all of the processing modules for hot spares or additional processing or test modules.

Below the main processing modules is a Gigabit Ethernet switch that handles communications between the System Controller and the individual processing module controllers. If required two of these units could be supplied for redundancy or CERN's in house networking switches could be used.

There are two System Controllers for redundancy. Each of these controllers will have twin, SCSI disks in a RAID configuration and run with identical software.



Rack System

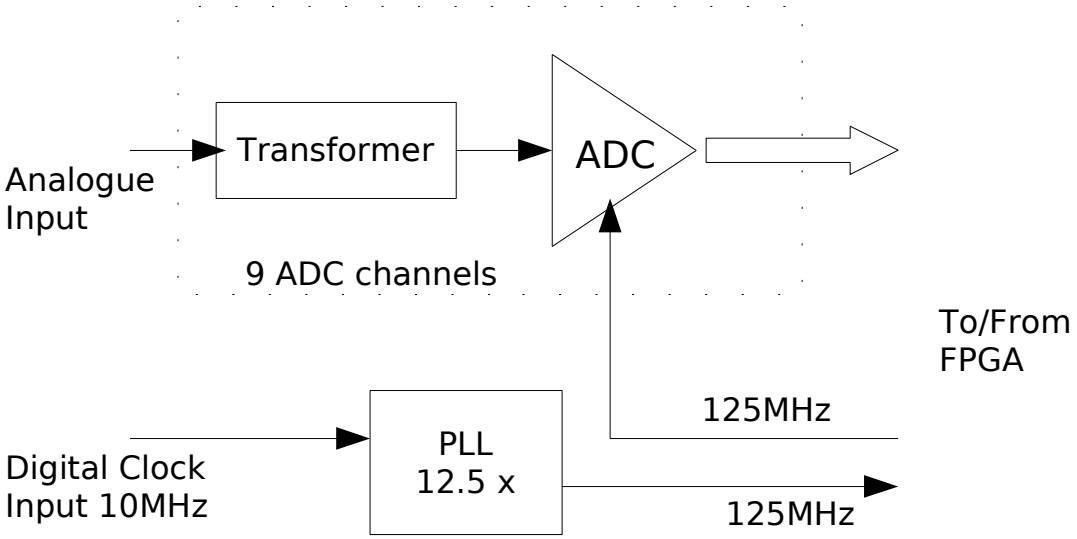
6. PU Processing Engine

The complete system has 17 PU processing engines each housed on a cPCI board. Fourteen PU processing engines are needed to support the 40 PU's and three boards are available as cold or hot spares. The PU processing engine consists of a custom cPCI carrier board on which is mounted the ADCs and digital I/O interface components. There is a PMC site on this carrier board into which is plugged an Alpha Data COTS FPGA module which implements the data processing.

The design makes full use of the Virtex-4 FPGA to provide a flexible hardware design solution that can be tailored in the FPGA firmware design.

6.1. PU ADC Front End

The data acquisition front end has nine 125 MS/sec 14 bit analogue to digital converters. The ADC chip used will probably be the Linear Technology LTC2255, although the actual device decision will be determined during the main system design phase. The ADC's are fed from the input connectors via isolating transformers. The isolating transformer will probably be the MCL AT1-6T which has a 1dB bandwidth of 50kHz to 50MHz. The isolation transformer reduces the possibility of problems due to the complex systems involved in the complete Proton Synchrotron. A separate digital clock input is provided that can accept the systems 10 MHz master clock or perhaps a 125 MHz sample clock. The ADC front end has a, low jitter, PLL for the generation of the ADC sample clock and FPGA processing clock from the incoming clock signal. We expect to use the ICS601-02 PLL which has a low jitter of a few 10's of pico seconds. As the clock generation is controlled by the main FPGA, the actual ADC clock can be generated directly by the FPGA or be routed from the systems timing bus if required for test purposes.



ADC Input Channels

The input connectors will be SMA. The input impedance will be 50 ohm's and the full scale ADC range will be 1 Volt peak to peak.

There will be no anti-aliasing filters prior to the ADC's as CERN's current PU and pre-amplifier combination already perform this function.

6.2. PU Digital I/O Front End

The PU processing engines carrier board will provide 16 digital input/output channels. On each individual PU engine board 1 digital input and 3 digital output channels will be available through SMA connectors. The rest of the 16 digital input/output channels will be available on a sockets on the board that can be connected to a nearby panel containing SMA connectors. The first PU engine board in a processing module will have such a digital I/O panel next to it to support the 8 Trajectory Measurement System digital input synchronisation signals.

The digital inputs and outputs will be TTL compatible with a 50 ohm characteristic impedance. These signal lines will be connected to the on-board FPGA through which they may be routed to/from the cPCI backplanes timing bus or used directly by the FPGA.

The three digital outputs, on each processing engine, will be able to be configured to output test signals from the PU processing engines. It is expected that the re-constructed Fref will be available on these connectors.

6.3. FPGA Processing Engine

The FPGA processing engine is a standard Alpha Data PMC COTS component. The proposed part is the Alpha Data **ADM-XRC/FX100-10/1G**. This module is a PMC module the data sheet for which is enclosed with the tender. The FPGA is a Xilinx Virtex-4-FX100, one of the latest Xilinx chips available and has 1 GBytes of DDR-II RAM in four banks connected to it. The FPGA is connected to the ADC's and digital I/O on the cPCI carrier. A secondary FPGA on the PMC module implements a PCI bus to local bus bridge which connects the main data processing FPGA with the cPCI bus. This provides communications between the main FPGA and the processing module's controller via the cPCI carrier board and the cPCI backplane.

The timing bus on the cPCI backplane is also connected through to the FPGA. This allows the external digital timing signals which are passed along the cPCI backplane to be routed through to the main FPGA. It also allows the digital I/O signals to be routed through to the cPCI backplane's timing bus.

The Xilinx Virtex-4 FX100 device has around 100,000 Logic cells and has 6,768 kbits of RAM. It also has 160 special DSP slices as well a many other features. It will easily have sufficient capacity to deal with the algorithms specified in CERN's technical documentation for 3 PU's and has spare capacity for future processing developments to match CERN's research and development role. The FPGA also includes two embedded 32 bit Power PC processors. These could also be used in future system developments by CERN.

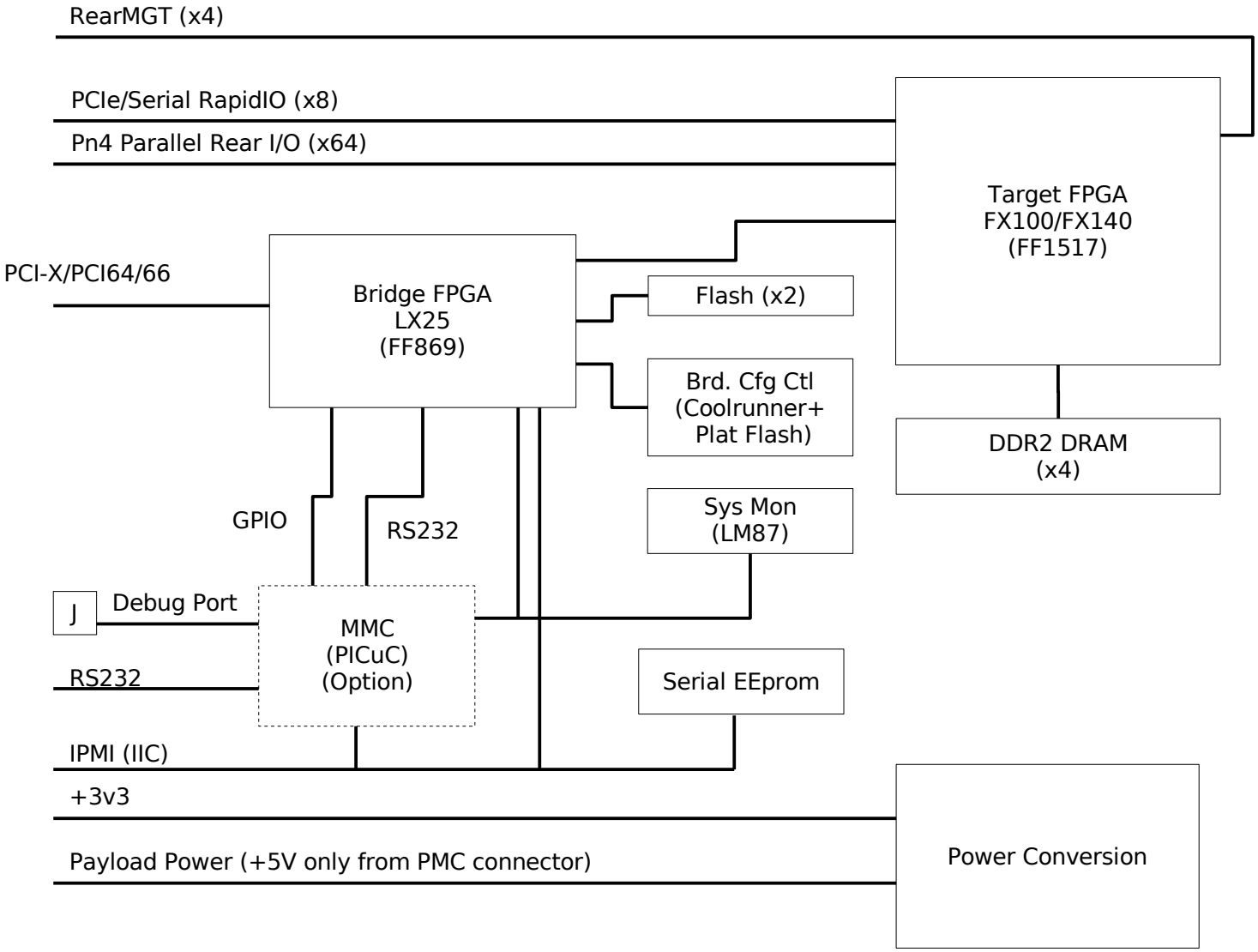
The DDR-II memory interface has a peak data rate of 6.4GB/sec and so will easily cope with the 3 x 120 = 360 Mbytes/sec of data input together with requests for data output.

During the main system design phase we may decide to build the FPGA processing engine directly on the cPCI carrier board rather than use a separate PMC module. In this case the FPGA design will be the same as used in the **ADM-XRC/FX100-10/1G** PMC module**.**

The FPGA will probably be booted from the processing modules controller, however it is also possible to load the FPGA code from on-board FLASH memory if required.

The FPGA has on board Gigabit Ethernet controllers, but no Ethernet PHY interface chips. An alternative system design could replace the cPCI bus with a direct Gigabit Ethernet connection if required.

The designs FPGA solution provide huge power and flexibility for future processing needs.



ADM-XMC-4

7. Processing Module

Each processing module is independent of other processing modules. It consists of an 8 way cPCI backplane with power supply, a conventional CPU based module controller and 4 or 5 PU processing

engines.

7.1. Module Controller

The module controller will be a COTS component. It will have a conventional CPU, some boot FLASH memory, 1 Gigabyte of RAM, a cPCI bus interface and dual Gigabit Ethernet ports. The actual unit to be used will be decided during the main design phase. A possible unit is the Concurrent Technologies PP 332/020. This is based on a low power Pentium M processor.

The module controller will boot from the main system controller over the Ethernet interface and will run a small Linux based operating system. It will be responsible for booting and managing the 5 PU processing engines (15 Proton Synchrotron PU's). Communications between the system controller and the individual PU processing engines will also be handled.

It will also be responsible for loading the PU processing engines "event switch table" for each processing cycle.

8. System Controller

The system controller will be a standard Intel Pentium based computer system. It will probably be housed in a separate 2U or 4U 19" rack enclosure although it may also be implemented as a cPCI controller card similar or indeed the same as the module controllers. The system controller will have 1 Gigabyte of memory and dual disk drives in a RAID configuration for disk redundancy. These disks will contain all of the system's software, FPGA firmware and configuration information. The controller will have dual Gigabit Ethernet interfaces, one connected to the Gigabit switch that communicates with the processing module's controllers and one connected to the sites LAN for remote access to the system.

The system controller will not have a monitor, keyboard or mouse although these could be provided if required. All system configuration and maintenance will be carried out over the Ethernet network. The system controller will run the Linux operating system.

Two identical system controllers will be provided for system redundancy. It has yet to be decided how best to implement the switch over between the two controllers in the event of failure. This could be manual or automatic. We will consult with CERN during the main system design phase on this decision.

As well as providing a control and data interface to the Trajectory Measurement System, the software on the system controller will implement system boot, system configuration, system test and fault diagnostics functions. This will probably be made available to operators via a web based interface as well as through a command line API.

9. System Software and API's

All of the system software will be based on the Linux operating system. This will provide a reliable an

flexible system that can be easily maintained locally and remotely. All of the software will Open Source and thus all source code will be available. All of the system's special software will be available in source code form with an Open Source license.

All communications will be through the system controller which will support a simple, API to control and gather data from the system. The system controller will interrogate the individual PU processing engines via the local Gigabit Ethernet network and the module controllers. CERN can control and acquire data across the network interface from a remote system via the network based API or install their own programs on the system controller which will communicate with the system using the same API.

The system controller will accept "cycle control packets" from CERN's system describing each Proton Synchrotron's machine cycle. This information will allow the data captured to be tagged with the appropriate cycle information. This information will be sent to all of the PU processing engines along with configuration data such as the position of the PU engine within the Proton Synchrotron's ring.

Individual information tables will be distributed to each of the PU processing engines by this software using CERN's supplied data.

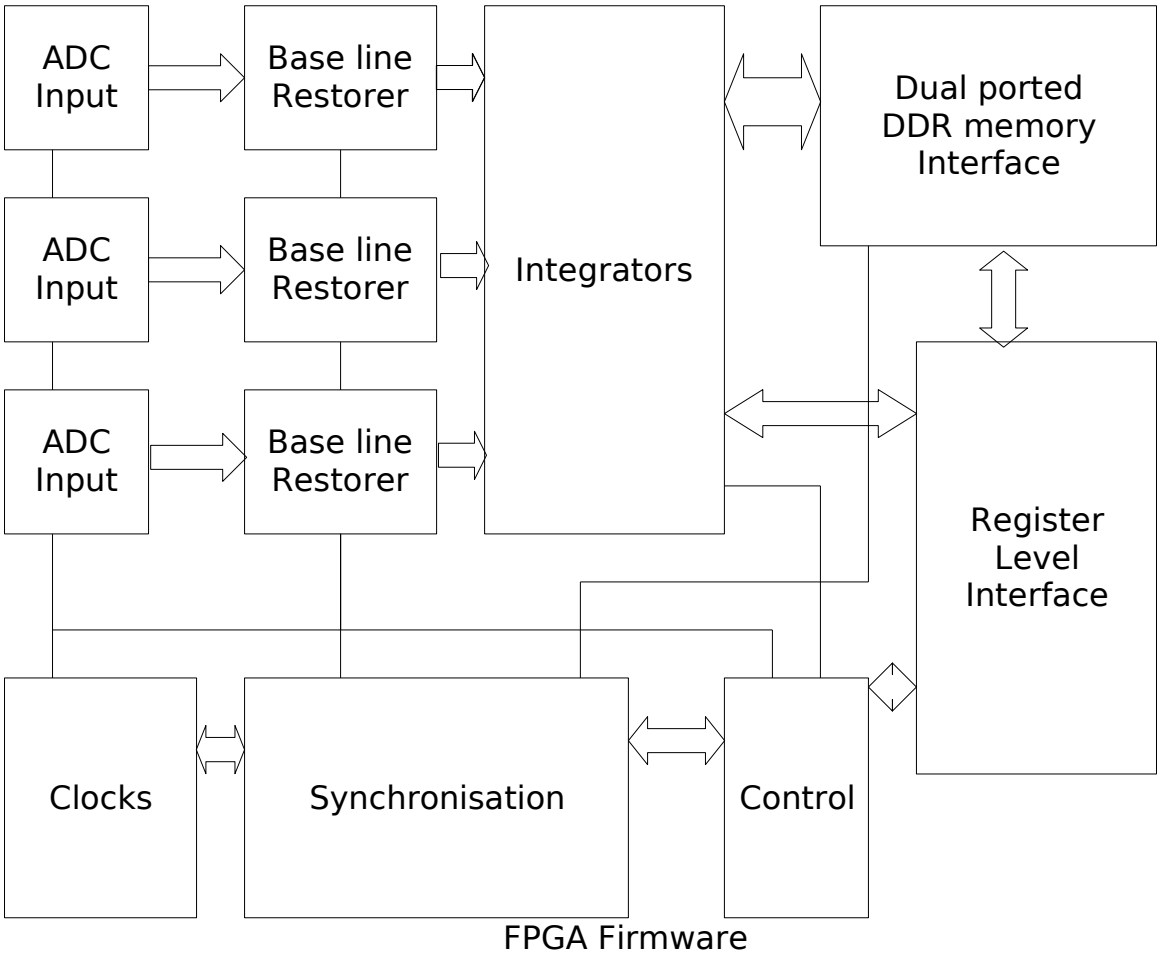
The system controller will be able to handle the swapping of hardware modules due to failure without any changes needed to CERN's control information.

The full design of the system software will be carried out during the system design phase and will involve detailed discussions with CERN for more detail on requirements.

The software will be developed on the GNU/Linux operating system and the Open Source GNU tool-set will be all that is required to develop the software.

10. FPGA Firmware

The FPGA firmware will be developed using the Xilinx ISE Foundation tool-set in the VHDL language. Alpha Data's engineers have a great deal of experience in implementing various DSP type designs ont FPGA fabric.



Some of the FPGA firmware blocks are available as standard Alpha Data IP. This includes the base of the register level interface, the DDR memory interface and the ADC input interface. The rest of the FPGA firmware will be developed following the algorithms in CERN's technical specification. The DDR memory in the FPGA is physically split into 4 banks. We expect to use one bank per PU channel (256 MByte) and to use the fourth RAM bank for the synchronisation tables and or test signals. The synchronisation tables may also reside in FPGA on-chip RAM instead of the DDR memory.

The FPGA firmware will include diagnostics and test functions including those specified in CERN's technical specification.

The FPGA firmware will be made available to CERN in VHDL source form so that CERN could modify and extend the system at a later date if required.

11. System Testing

As part of the tender we have costed in producing a test signal generator. This will produce simulated versions of the three PU signals and the main digital timing signals. This system will be used to simulate

the real CERN Proton Synchrotron system. We understand that CERN has suitable signal data that we can use to produce the appropriate signals.

The test signal generator will be used during the development of the hardware, FPGA firmware and host software of the system as well as for primary system testing. It will also be used during the maintenance and support phase so that we have a simulated CERN Proton Synchrotron system which will help with support.

After the initial support/maintenance phase, it will be possible to ship this test signal generator to CERN for system test, development and calibration purposes if required.

After the pre-series unit has been shipped to CERN, testing with real the Proton Synchrotron system will be performed at CERN's site. This will be carried out with Alpha Data and CERN's technical engineers present.

12. System Parts

This lists the high level parts we have based our tender on. During the real system design phase, changes may be made to the components used.

Qty	*COTS*	*Part*	*Description*
2	yes	Bustronic 6U backplane in 9U cPCI rack unit	This is the 8 + 8 slot 19inch 9U rack enclosure and power supplies for the processing modules.
4	yes	PP 332/020	A cPCI CPU controller board.
17	no	ADC and Digital I/O PMC cPCI carrier board	On each of these cPCI boards an FPGA processing engine in PMC form factor will be mounted..
17	yes	ADM-XRC/FX100-10/1G	FPGA data processing PMC module.
1	yes	Netgear GS116	Gigabit Ethernet Switch.
2	yes	Boston Supermicro server	System Controller.

13. Internet Links for Components

Some Internet web links for the major component parts are given below:

Item	*Link*
Alpha Data FPGA boards	http://www.alpha-data.com
LTC2255 ADC	http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1001,C1150,P11912

Item	*Link*
Xilinx Vertex-4 FX100	http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/index.htm
Compact PCI controller card	http://www.cct.co.uk/sheets/pp33202x.htm
Bustronic backplanes	http://www.elma-mektron.co.uk/

14. Deliverables

We will ship the following items to CERN during the contract.

Date	*Description*
30th November 2006	The pre-series unit will be shipped to CERN for testing. This will consist of: 1 processing module, 1 Gigabit Ethernet switch and 1 System controller. The processing module will contain: 1 cPCI backplane with 1 processing module controller and 1 PU processing engine (3 Proton Synchrotron PU's). Preliminary documentation will be available on a support web site and if requested in paper form. We will visit with the system and perform initial testing with the Proton Synchrotron and demonstrate its use to CERN's staff.
19th March 2007	The full series units will be delivered to CERN.
30th March 2007	We will visit CERN to install and commission the full system. During this visit we will provide a 3 day training session to CERN's staff on the use and maintenance of the system. We will also deliver the following: Full documentation on CDROM/DVD. FPGA firmware in binary and source code forms. Software on CDROM/DVD in binary and source code forms. All documentation, FPGA firmware and software will also be available on a support web site and if requested in paper form.

15. Project Management

The project time-scales are quite tight, especially in the early stages, so keen project management will be

required. Alpha Data shall insure that this in place at the start of the contract by appointing a single project manager for the overall project.

In order to improve communications between the parties, designers and developers involved in the contract we will set up a secure web-site at the start of the contract to disseminate live information on the project. This will provide all technical documents, email communications, project notes and project status. All training support materials will be placed on the support web site so that CERN's support engineers can access the information at any time. We have found with numerous similar projects, this type of system helps keep projects on time and to budget.

As the project progresses system software and FPGA firmware will be available on this web site as well as final system documentation. The site will continue to function during the support an maintenance phases.

We will arrange visits to CERN or from CERN of key people involved in the project in the early and later stages of the project. We will provide, at least, monthly updates on the project's status to CERN's staff responsible for the project.

We perceive the main project risks to be:

- Hardware boards cannot be designed, developed and manufactured on time for pre-series unit. We have a backup plan using COTS components should this happen.
- CERN's proposed Trajectory Measurement System algorithms need some modification once the system has been tested on real data. We have included extra development time within the support and maintenance phases to handle this eventuality.

16. Time Scales

With the solution we propose there is a need to produce a custom hardware module and perform around 90 man days of FPGA firmware and software development. All of this will have to happen prior to having a working prototype (pre-series system). CERN has stated that no components should be purchased or hardware manufactured prior to CERN accepting the design, which will take 3 weeks. This means that assuming a 1 month main design phase, hardware development and production cannot begin until about 30th August 2006. Expected elapsed development time for the hardware modules is 3 months. FPGA firmware and Software development can be carried out in parallel during this time. This schedule makes it possible to deliver a pre-series unit by the 30th November 2006 but schedules are tight. As a backup plan, should there be un-avoidable large delays in the project, it will definitely be possible to produce a prototype unit working with two ADC channels using Alpha Data's COTS components for 30th November 2006. This will allow testing the FPGA algorithms with the Proton Synchrotron prior to its yearly shutdown period. Our tender also includes the production of a Proton Synchrotron test signal generator. We will provide CERN's staff with Internet access to the prototype system so that they can run their own tests

on the proto-type if required during the development period.
A provision schedule of work is as follows:

Date	Work to be done
10th July 2006	Contract start date. System design work. 1 months. Set up secure support web site during this stage.
11th August 2006	Send system design send to CERN for approval. Start work in background on hardware design, FPGA firmware design and software design. Keep checking with CERN to see if system system design is acceptable. System test signal generator will be designed and built during this stage.
30th August 2006	CERN gives go-ahead for the system design. Work continues on hardware design, FPGA firmware design and software design. Development of hardware, FPGA firmware and software starts. System COTS components are purchased for pre-series working prototype. During this stage standard COTS hardware can be used for development purposes.
30th October 2006	Hardware prototypes will be built and will be tested. Any necessary hardware re-works are implemented. Development of hardware, FPGA firmware and software continues.
17th November 2006	Basic FPGA firmware and basic host software has been implemented and can be tested on the prototype system hardware which will now be available. Testing and further development on the FPGA firmware and software continues. Start on developing system diagnostics software to aid support and maintenance. Provisional system documentation is produced.
30th November 2006	Pre-series working prototype available for testing. Start testing pre-series system.

Date	Work to be done
	Visit by CERN to install pre-series working prototype and assist with setting up and testing. Further development on the FPGA firmware and software continues.
15th December 2006	CERN gives agreement for production of full series units. Production work on full series units starts. Further development on the FPGA firmware and software continues.
28th February 2007	Series working units available. Testing and development continues.
19th March 2007	Installation at CERN of the full system commences.
30th March 2007	Installation and commissioning completed and ready for acceptance testing.
1st April 2007 onwards	System support, bug fixing and maintenance.

17. Initial 3 years Support and Maintenance

The preliminary system design is based on a modular approach with a large degree of common modules and redundancy of the main system components. This system will also have self diagnostics, information from which will be available to CERN's staff. Also, if possible through CERN, we could also remotely monitor the diagnostics information via a secure Internet based interface. We will train CERN's staff to be able to use the diagnostics to ascertain if there is a problem and to be able to swap modules. This will reduce system down time to a minimum in the event of a fault.

We have costed in the provision of a 3 day training course that can be held at CERN's premises or at our premises in Edinburgh. One of our design engineers will give this training course and will be fully conversant with the system. We will use the spare system and test signal generator to simulate the real system during this training. All training support materials will be placed on the support web site so that CERN's support engineers can access the information at any time.

We will provide email, fax and telephone support to CERN's engineers to assist with problems. In the case of a fault where the fault cannot be rectified by email/telephone support or the swapping modules, we will expect to be able to fly out an engineer to CERN with replacement parts within 24 hours of a call. This will be restricted to normal working days and will depend on the availability of flights to Geneva from the UK. We have included up to 9 man days on-site support to sort out these faults.

We have included 3 man days to provide a yearly maintenance visit during the yearly shut down period. During this visit we will clean the systems air ventilation pathways and check the system over using a test signal generator.

We will support a secure, Internet based, web site that will provide all system documentation, fault finding flow charts and other information to aid maintenance of the system.

We have included in the maintenance and support costs keeping a small set of system components, in addition to the spares held at CERN. These will provide us with a cut-down system which we can use to assist us in tracking down system faults and fixing them. Also, we can use these parts to replace the spares at CERN should these fail. If additional components are required outside of the guarantee period we can supply these, subject to component availability, at the appropriate retail price.

We have also included 16 man days FPGA and software development time in the support and maintenance cost. We understand that CERN is a research establishment and that CERN's technical specification for the Trajectory Measurement System may need some changes once the algorithms are used on a real Proton Synchrotron system. This development time should cover minor changes to the system.

We can provide a maintenance plan for up to ten years after commissioning. With this plan, as part of the yearly maintenance visit, we will change the system's disk drives for new units every 3 years and every 5 years we will change the systems main fans. Please contact us for more details.

18. Conclusions

There are many possible design options for the CERN Trajectory Measurement System. One option we considered was using one FPGA per PU channel. This would be slightly more modular, but would be more costly as the major component cost is the FPGA itself. Described in this document is a provisional design that we believe best matches CERN's requirements for now and provides excellent extra features for possible future developments. However, we are open to designing the system in a different way if required. The system with just firmware and software modifications would be suitable for many other high performance, real-time, instrumentation systems at CERN.