Idea for Phase/Switch Table

Name	*Bit*	*Description*
FRefSel	0	Selects the FREF timing input or the ADC Sigma as the frequency reference to lock on-to. This changes the both the input reference source, and which of PllFRef or PllFRefHarmonic to use as the feed back signal in the PLL.
PllFRef	1	Phase table to synchronise to FREF
PllFRefHarmonic	2	Phase table to synchronise to Harmonic number * FREF ie Sigma
Gate	3	Gate signal for data integration
Blr	4	Base line restore signal
Acquire	5	Acquire data signal
Spare0	6	
Spare1	7	

There would be 16 Phase tables. Each would have 512 x 8bit entries. Thus the memory requirement would be 16 x 512 bytes.
On each timing signal the table would switch to the next table in the 16 table array. Instead of this simple method of Phase table change, we could have a separate timing signal selection switch table to choose which signal would effect a Phase Table change or even include this in the main Phase/Switch tables.