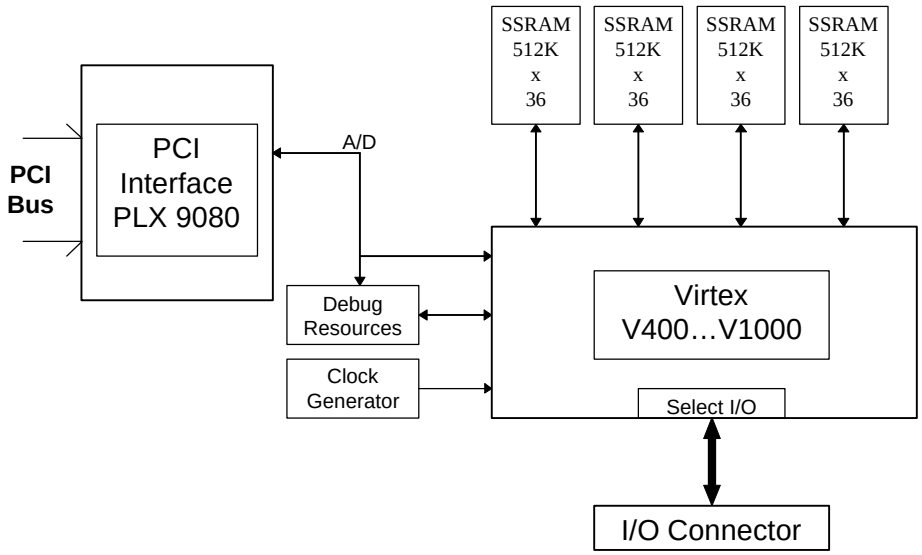
ALPHA DATA *parallel systems ltd*

ADM-XRC (Xilinx Reconfigurable Computer)

Specification

- Industry standard PMC format
- Support for the largest Virtex devices from V400 to V1000 and VirtexE to 2000E
- High speed PCI bus interface using PLX9080 not in FPGA
- 4 banks of 256k/512k x 36 bits of synchronous, Syncburst/ZBT SRAM
- Programmable clock generator
- Support for Xilinx BoardScope® for debugging
- On board re-programmable flash memory for embedded configuration
- High density I/O connector in standard SCSI-2 format
- Virtex / VirtexE power supplied on board



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PCI Bus	Revision 2.1 Compliant 3.3V or 5V I/O Twin DMA channels support actual data rates of 116Mbytes/sec to Virtex.
Flash	2MByte, programmable in-circuit
FPGA	Xilinx Virtex XCV400/600/800/1000-4/5/6-BG560 VirtexE up to XCV2000E when available
SRAM	Standard 100 pin TQFP can support ZBT or equivalent or synchronous burst. Flow through or pipelined types. 8Mb 256k x 36 16Mb 512k x 36 optional
Configuration	PCI Bus direct to SelectMAP port for fast configuration From Flash direct on power up External JTAG connector
SelectMap	Configuration port supports direct access to Virtex configuration for download or readback. DMA can be used to configure at up to 30Mbytes/sec. Support for Xilinx BoardScope®.
JTAG	A standard JTAG port is provided that can be used for programming both the Virtex FPGA and CPLD support logic for debugging or firmware upgrade.
Clocks	On board clock generator provides a synchronous local bus clock for the PCI interface and the Virtex FPGA. A second clock is provided to the Virtex FPGA for user applications and can be free running or stepped under software control. Both clocks are programmable and can be used by the Virtex Clock DLL functions:- **Local Bus** 400kHz to 40 MHz **User Clock** 0Hz to 100MHz
External I/O	34 I/O lines from FPGA Bank
Power Consumption	5V @ 600mA 3.3V @ 1200mA

Ordering Information

ADM-XRC/xxxx/y/z With Vxxxx(-y) and z Mbytes of ZBT SSRAM
xxxx - 400 / 600 / 800 / 1000 / 1000E / 2000E
y - 4 / 5 / 6
z - 4 / 8

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