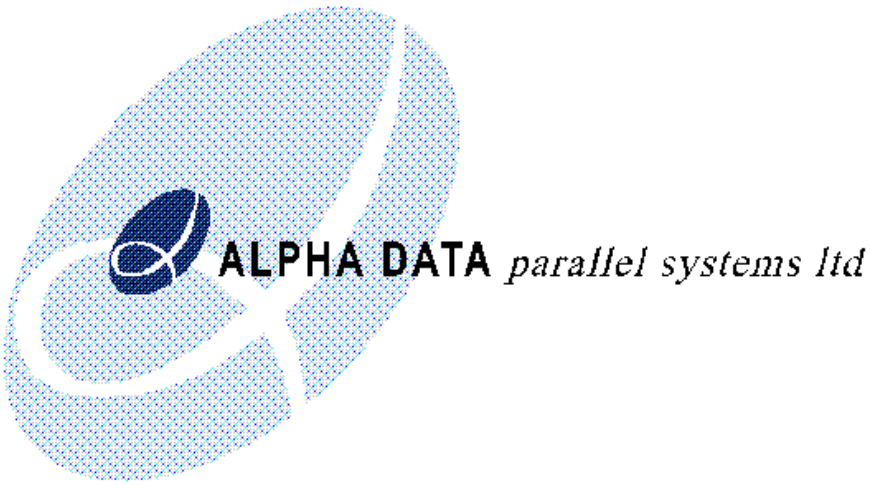
ALPHA DATA *parallel systems ltd*

ADC-PMC-64
User Manual



Version 1.1

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Important Note

This manual describes the functions available in the ADM-XRC Support Software Library.

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1. Introduction

1.1. About the Hardware

The ADC-PMC is a 64-bit PCI carrier card for PMC modules. It can be used in 3V and 5V signalling environments and in both 32 and 64-bit slots. There are two PMC slots on the standard card and these can also support 32 or 64-bit operation. The secondary bus VIO can be configured in the factory for 5V or 3V operation.

The ADC-PMC carrier card also supports features of the ADM-XRC FPGA board in a PCI environment with the provision of Pn4 routing between the two PMC sites and selectively to a 64-way header.

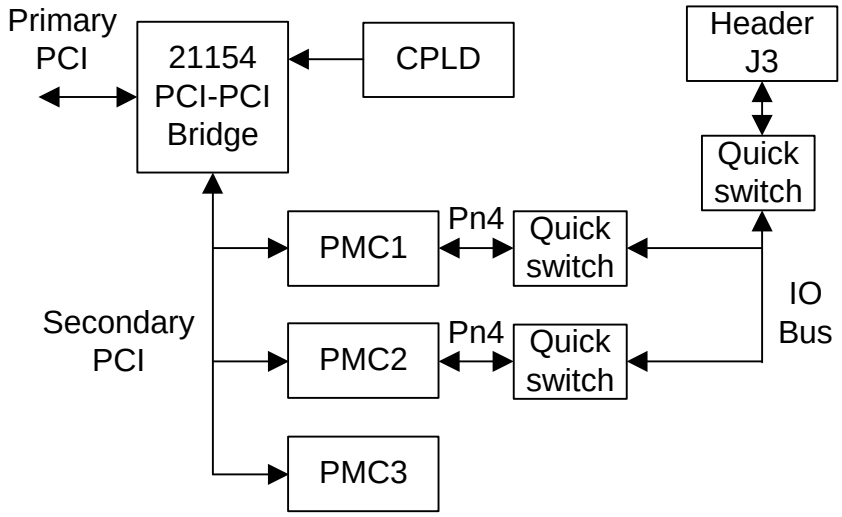
Both primary and secondary bus interfaces are rated at up to 33MHz operation.

1.2. Description

The ADC-PMC is based on the 21154 64-bit PCI-PCI bridge manufactured by Intel. This device supports 64 or 32 bit primary PCI and 64 or 32-bit secondary PCI.

The ADC-PMC provides two PMC sites with an optional third site for debug purposes. Each of the two primary PMC sites supports Pn4 IO with quick-switch isolation to permit various IO combinations. A set of jumpers on the board enables each of the quick-switch blocks.

The IO-Bus is 64 bits wide and connects to all 64 signals from the Pn4 connector of each PMC site. Further, a subset of the IO-Bus can be routed to the J3 header through a quick-switch block that provides a level of protection to the IO bus signals by limiting the external signal levels.



2. Installation

In order to ensure that the board operates correctly first time, please read these instructions completely before attempting installation. It will also help you to read the whole manual first so that you know how you want the board to be set up. Figure 1 shows the physical layout of the board. The installation instructions for your PC should be followed at all times.

2.1. Into a PC

The ADC-PMC is a universal PCI device meaning that it can be used in both 3V and 5V signalling environments.

2.2. Adding PMC cards

Fit any PMC modules that are required. If only one PMC module is to be fitted, either site can be used. PMC site #1 is positioned so that an I/O connector on the module aligns with the aperture in the ADC-PMC's edge panel. The PMC modules should be supplied with mounting kits, which normally include spacers, nuts, bolts and washers. Figure 1 shows the typical assembly of a PMC to the ADC-PMC. It is recommended that washers be used on both sides of the ADC-PMC to avoid damage to the PCB.

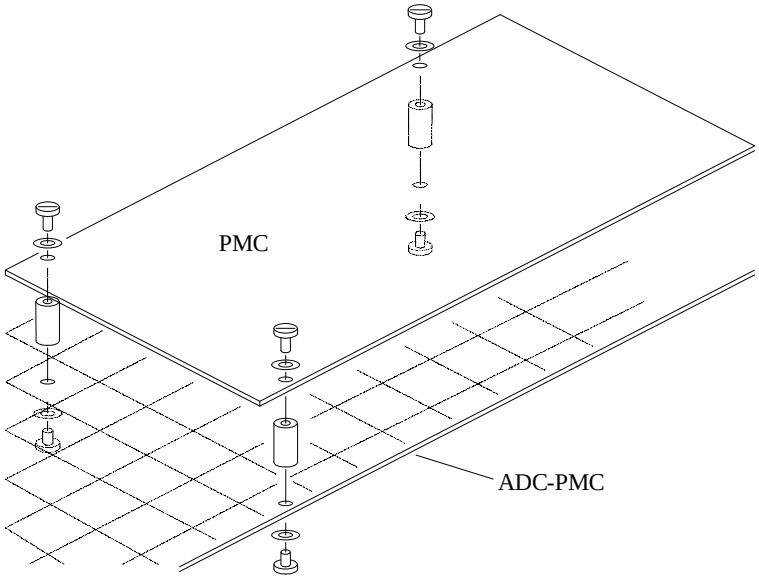


Figure 1 Assembly of a PMC to the ADC-PMC

2.3. Software Support

The ADC-PMC uses an Intel 21154 64-bit bridge device that is compatible with most operating systems that adhere to the PCI Bios specification.

No software is required to enable operation of the ADC-PMC.

3. Hardware Pin-out Information

3.1. Jumpers

There are 10 jumper sites on the board that are used for configuration settings.

Jumper	Usage	Fitted	Not Fitted
J1	Secondary PCI bus clock select	33MHz PMC Bus	Auto select PMC clock
J2	PMC1 Monarch	Not supported	
J3	Option1	PMC1 Pn4 connected to IO bus	PMC Pn4 isolated
J4	PMC2 Monarch	Not supported	
J5	Option2	PMC2 Pn4 connected to IO bus	PMC2 Pn4 isolated
J6	PMC3 Monarch	Not supported	
J7	Option3	Header J3 connected to IO bus	Header J3 isolated
J8	Option4	Not supported	
J9	Option5	Not supported	
J10	Option6	Not supported	

Notes.

- J1 should always be fitted on ADC-PMC Revision 1.
- J2, J4, J6 and J8-10 are reserved for future use. Do not fit links in these positions.
- J3, J5 and J7 can be fitted in any combination. Check the Pn4 information for the PMC's that are fitted to ensure there are no contention issues.

3.2. J1 PCI Connector

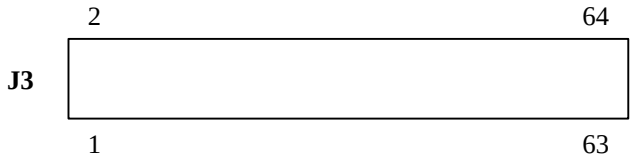
This is a standard edge connector for PCI and is compatible with 32-bit slots with 3V or 5V signalling and 64-bit slots with 3V signalling.

3.3. J2 JTAG Connector

This connector provides access to the CPLD, U2, and should only be used in manufacturing as changes to this device could cause system failure.

3.4. J3 Header Configuration

The IO header, J3, is suitable for mating with IDC connectors or Berg based crimp terminals.



gnd	1	2	hdr_io0
hdr_io1	3	4	hdr_io2
hdr_io3	5	6	gnd
hdr_io4	7	8	hdr_io5
hdr_io6	9	10	hdr_io7
gnd	11	12	hdr_io8
hdr_io9	13	14	hdr_io10
hdr_io11	15	16	gnd
hdr_io12	17	18	hdr_io13
hdr_io14	19	20	hdr_io15
gnd	21	22	hdr_io16
hdr_io17	23	24	hdr_io18
hdr_io19	25	26	gnd
hdr_io20	27	28	hdr_io21
hdr_io22	29	30	hdr_io23
gnd	31	32	hdr_io24
hdr_io25	33	34	hdr_io26
hdr_io27	35	36	gnd
hdr_io28	37	38	hdr_io29
hdr_io30	39	40	hdr_io31
gnd	41	42	hdr_io32
hdr_io33	43	44	hdr_io34
hdr_io35	45	46	gnd
hdr_io36	47	48	hdr_io37
hdr_io38	49	50	hdr_io39
gnd	51	52	hdr_io40
hdr_io41	53	54	hdr_io42
hdr_io43	55	56	gnd
hdr_io44	57	58	hdr_io45
hdr_io46	59	60	hdr_io47
gnd	61	62	hdr_io48
hdr_io49	63	64	gnd

3.5. ADM-XRC/P to J3 Header Configuration

The ADC-PMC is usually provided to support ADM-XRC cards of both front and rear (Pn4) types. An ADM-XRC/P with Pn4 IO can be used on the ADC-PMC-64, typically to communicate with another ADM-XRC/P. The Pn4 signal set can be routed to J3 on the ADC-PMC to provide debug or prototyping access to the ADM-XRC FPGA.

The current revision of the ADC-PMC supports up to 50 I/O signals on J3 and the actual amount available will vary depending on the type of ADM-XRC fitted.

The table below shows the J3 configuration with a Revision 1 ADM-XRC/P providing 43 IO signals.

	gnd	1	2	hdr_io0	user[0]
user[1]	hdr_io1	3	4	hdr_io2	user[2]
user[3]	hdr_io3	5	6	gnd	
user[4]	hdr_io4	7	8	hdr_io5	(gnd)
user[5]	hdr_io6	9	10	hdr_io7	user[6]
	gnd	11	12	hdr_io8	user[7]
user[8]	hdr_io9	13	14	hdr_io10	user[9]
user[10]	hdr_io11	15	16	gnd	
user[11]	hdr_io12	17	18	hdr_io13	user[12]
user[13]	hdr_io14	19	20	hdr_io15	user[14]
	gnd	21	22	hdr_io16	(gnd)
user[15]	hdr_io17	23	24	hdr_io18	user[16]
user[17]	hdr_io19	25	26	gnd	
user[18]	hdr_io20	27	28	hdr_io21	user[19]
user[20]	hdr_io22	29	30	hdr_io23	user[21]
	gnd	31	32	hdr_io24	user[22]
user[23]	hdr_io25	33	34	hdr_io26	user[24]
(gnd)	hdr_io27	35	36	gnd	
user[25]	hdr_io28	37	38	hdr_io29	user[26]
(gnd)	hdr_io30	39	40	hdr_io31	(gnd)
	gnd	41	42	hdr_io32	user[27]
user[28]	hdr_io33	43	44	hdr_io34	user[29]
user[30]	hdr_io35	45	46	gnd	
(gnd)	hdr_io36	47	48	hdr_io37	user[31]
user[32]	hdr_io38	49	50	hdr_io39	user[33]
	gnd	51	52	hdr_io40	user[34]
user[35]	hdr_io41	53	54	hdr_io42	user[36]
user[37]	hdr_io43	55	56	gnd	
user[38]	hdr_io44	57	58	hdr_io45	user[39]
user[40]	hdr_io46	59	60	hdr_io47	user[41]
	gnd	61	62	hdr_io48	user[42]
(gnd)	hdr_io49	63	64	gnd	

(gnd) is a ground from the ADM-XRC Pn4 connector routed to the header. Do not use as a ground as this signal may support user IO in future.

4. Revision History

Date	Rev	Comment
July-2001	1.1	Updated section 3.5 to map user[5] and user[6] correctly