Register Map and Descriptions

Table 3-1. PCI-6110E Register Map

Register Name	Offset Address		Type	Size
	Hex	Decimal		
Misc Register Group				
Serial Command	0D	13	Write-only	8-bit
Misc Command	0F	15	Write-only	8-bit
Magic	19	25	Write-Only	8-bit
Status	01	1	Read-only	8-bit
Calibration Channel Select	1A	26	Write-only	16-bit
Analog Input Register Group				
ADC FIFO Data Register	1C	28	Read-only	32-bit
Configuration Memory Low	10	16	Write-only	16-bit
Configuration Memory High	12	18	Write-only	16-bit
AI FIFO Offset Load	5	5	Read-only	8-bit
Analog Output Register Group				
AO Configuration (NOT SUPTED)	16	22	Write-only	16-bit
DAC FIFO Data	14	20	Write-only	32-bit
AO Window addr Register	18	24	Write-Only	16-bit
AO Window Data Register	1E	30	Write-Only	16-bit
DAC0 Direct Data	W(0-F)	W(0-15)	Write-only	16-bit
AO Update time	W 10	W16	Write-only	16-bit
AO Update Imm	W 11	W17	Write-only	16-bit
AO FIFO Offset Load	W 13	W19	Write-only	16-bit
AO later internal	W 14	W20	Write-only	16-bit
AO WG Register	W 15	W21	Write-only	16-bit
AO Misc Register	W 16	W22	Write-only	16-bit
Cal Gain Select Register	05	5	Write-only	8-bit
AI AO Select	09	9	Write-only	8-bit
G0 G1 Select	0B	11	Write-only	8-bit
DAQ-STC Register Group				
Window Address	0	0	Read-and-write	16-bit
Window Data	2	2	Read-and-write	16-bit
Interrupt A Acknowledge	4	4	Write	16-bit
Interrupt B Acknowledge	6	6	Write	16-bit
AI Command 2	8	8	Write	16-bit
AO Command 2	A	10	Write	16-bit
G0 Command	C	12	Write	16-bit
G1 Command	E	14	Write	16-bit
AI Status 1	2	2	Read	16-bit
AO Status 1	4	4	Read	16-bit
G Status	6	6	Read	16-bit
AI Status 2	8	8	Read	16-bit
AO Status 2	A	10	Read	16-bit
DIO Parallel Input	C	12	Read	16-bit

Serial Command Register

The Serial Command Register control the PCI-6110E serial EEPROM and DACs. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 0D (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	**SerDacLd1**	**SerDacLd0**	**EEPromCS**	**SerData**	**SerClk**

Bit	Name	Description
7–5	Reserved	Reserved—Always write 0 to these bits.
4	SerDacLd1	Serial DAC Load1—This bit is used to load the second set of serial DACs with the serial data previously shifted into the DACs
3	SerDacLd0	Serial DAC Load0—This bit is used to load the first set of serial DACs with the serial data previously shifted into the DACs.
2	EEPromCS	EEPROM Chip Select—This bit controls the chip select of the onboard EEPROM used to store calibration constants. When EEPromCS is set, the chip select signal to the EEPROM is enabled.
1	SerData	Serial Data—This bit is the data for the onboard serial devices—the calibration EEPROM and the serial DACs. This bit should be set to the desired value prior to the active write to the SerClk bit.
0	SerClk	Serial Clock—This bit is the clock input to the two onboard serial devices. In order to write to these devices, this bit should be set first to 0 and then to 1. The data in the SerData bit will be written to the devices on the low-to-high transition of the serial clock.

Misc Command Register

The Misc Command Register contains one bit that controls the PCI-6110E analog trigger source. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 0F (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
Int/Ext Trig	***Trig1 AC/DC***	Reserved	***ATRIG1***	***ATRIG0***	**SCXI Enable**	**PFI7 DIR**	**LW FIFOEN**

Bit	Name	Description
7	Int/Ext Trig	Internal/External Analog Trigger—This bit controls the analog trigger source. If this bit is set, the output of the amplifier is selected as the trigger source. If this

bit is cleared, the TRIG1 signal from the I/O connector is selected as the trigger source.

6	Trig1 AC/DC	Trig1 AC/DC coupling bit - If this bit is set then AC coupling is enabled for the external analog trigger. If this bit is cleared DC coupling is selected.
5	Reserved	Reserved—Always write 0 to these bits.
4	ATRIG1	Analog Trigger 1 select - This bit controls which analog channel is used for the analog trigger.
3	ATRIG0	Analog Trigger 0 select - This bit controls which analog channel is used for the analog trigger.

ATRIG1	ATRIG0	Selected Channel
0	0	CH0
0	1	CH1
1	0	CH2
1	1	CH3

2	SCXI Enable	SCXI Enable - Write a 1 to this bit to enable SCXI operation. This effectively pulse extends the ScanClk and EXTGATECONV signals to meet SCXI requirements. Write a 0 this bit to enalbe flow through mode for those signals.
1	PFI7 DIR	PFI7 Dir bit - Write a 1 to this bit to make PFI7 an output, write a 0 to this bit to make PFI7 and input.
0	LW FIFOEN	Low Word FIFO Enable- This bit enable low word only FIFO writes. If this bit is set, only the low word FIFO gets data stored in it, if this bit is cleared both FIFOs are used.

Magic Register

The Magic Register contains misc bits to select different options for the PCI-611xE circuitry. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 19 (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**Overrun Enable**

Bit	**Name**	**Description**
7-1	Reserved	Reserved—Always write 0 to these bits.
0	Overrun Enable	Overrun Detection Enable bit - Write a 1 to this bit to turn off the overrun detection circuitry. This is useful if a user wants to run the board >5 MHZ so error interrupts (ie Overflow) can still be enabled in the DAQ-STC.

Status Register

The Status Register is used to indicate the status of various PCI-6110E resources..

Address: Base address + 01 (hex)
Type: Read-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
AILWEF*	**Temp OUT**	**AO PFF**	Reserved	Reserved	Reserved	Reserved	**PROMOUT**

Bit	Name	Description
7	AILWEF	AI Low Word Empty Flag - This bit indicated the status of the Empty flag for the AI Low Word FIFO. This bit is low if the LW FIFO is empty, high if data is present.
6	Temp OUT	Temperature Out - This bit reflects the serial output data from the temperature sensor.
5	AO PFF	AO Programmable Full Flag - This bit reflects the status of the AO programmable full flag. If this bit is set, the AO FIFO has (full - AO offset value) points or less stored in it.
4–1	Reserved	Reserved
0	PROMOUT	EEPROM Output Data—This bit reflects the serial output data of the serial EEPROM.

Cal Gain Select Register

The Cal Gain Select Register is used to calibrate the board on a per gain basis.

Address: Base address + 5 (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
7-0	D[7:0]	Data lines 7-0 - See table below to determine which values to write to calibrate at respective gains. The N1 value corresponds to the value which should be written to this register.

Input Range	Gain	N1	N2	Expected voltage
50	0.2	256	0	10.000000
20	0.5	256	0	10.000000
10	1	256	0	10.000000
5	2	249	7	9.453125
2	5	176	80	3.750000

1	10	152	104	1.875000
0.5	20	139	117	0.859375
0.2	50	132	124	0.312500

Calibration Channel Select Register

This register select which of the AI channels is to be calibrated.

Address: Base address + 28(hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CAL SEL1	CAL SEL0

Bit	Name	Description
15-2	Reserved	D<15..2> - Always Write 0
1	Cal Sel1	Calibration Select 1 - This bit selects the channel for calibration See table
0	Cal Sel0	Calibration Select 0 - This bit selects the channel for calibration See table

Cal Sel1	Cal Sel0	Selected Channel
0	0	CH0
0	1	CH1
1	0	CH2
1	1	CH3

Analog Input Register Group

ADC FIFO Data Register

The ADC FIFO Data Register returns the two oldest ADC conversion value stored in the ADC FIFO. Reading the ADC FIFO removes 2 values and leaves space for another ADC conversion value to be stored. Values are shifted into the ADC FIFO whenever an ADC conversion is complete.

The ADC FIFO is emptied when all values it contains are read. The empty, half-full, and full flags from the ADC data FIFO are available in a status register in the DAQ-STC. These flags indicate when the FIFO (32-bit) is empty, half-full, or full, respectively. Whenever the FIFO is not empty, the stored data can be read from the ADC FIFO Data register.

The values returned by reading the ADC Data Register are in two's complement binary, which generates both positive and negative numbers. Following is the bit pattern returned:

* To read the low word FIFO only, perform a 32 bit read from this register and discard the upper 16 bits.

Address: Base address + 1C (hex)
Type: Read-only
Word Size: 32-bit
Bit Map:

31	*30*	*29*	*28*	*27*	*26*	*25*	*24*
D31	***D30***	***D29***	***D28***	***D27***	***D26***	***D25***	***D24***
23	***22***	***21***	***20***	***19***	***18***	***17***	***16***
D23	***D22***	***D21***	***D20***	***D19***	***D18***	***D17***	***D16***
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
31–16	D<31..16>	Data bits 31 through 16—These bits are the result of the ADC conversion stored in the high word FIFO. The boards with a 12-bit ADC will return values ranging from -2,048 to 2,047 decimal (0xF800 to 0x07FF).
15–0	D<15..0>	Data bits 31 through 16—These bits are the result of the ADC conversion stored in the low word FIFO. The boards with a 12-bit ADC will return values ranging from -2,048 to 2,047 decimal (0xF800 to 0x07FF).

Configuration Memory Low Register

The Configuration Memory Low Register works with the Configuration Memory High Register to control the input channel selection multiplexers, gain, range, and mode settings. The values written to these registers are placed into the Configuration Memory, which is sequenced through during an acquisition. This register contains seven of these bits. The contents of the Configuration Memory are emptied by a control register in the DAQ-STC.

Address: Base address + 10 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
LastChan	Reserved	Reserved	GenTrig	Reserved	Reserved	DitherEn	Unip/Bip
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	**Gain3**	**Gain2**	**Gain1**	**Gain0**

Bit	Name	Description
15–10, 8–2	Reserved	Reserved—Always write 0 to these bits.

3-0	Gain<3..0>	Channel Gain Select 3 through 0—These three bits control the gain settings of the input PGIA for the selected analog channel. The following gains can be selected on the PCI-SMIO-5M:

Table 3-3. PGIA Gain Selection

Gain<3..0>	Range	Actual Gain
1001	±100	0.1
1010	±50	0.2
1011	±20	0.5
0001	±10	1
0010	±5	2
0011	±2	5
0100	±1	10
0101	± 0.5	20
0110	± 0.2	50
0111	NA	NA

*Not supported on the PCI-6110E

Configuration Memory High Register

The Configuration Memory High Register works with the Configuration Memory Low Register to control the input channel selection multiplexers, gain, range, and mode settings. This register contains nine of these bits. The contents of this register are cleared by a control register in the DAQ-STC.

Address: Base address + 12 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	**ChanType0**	**AC/DC***	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Bank1	Bank0	Chan3	**Chan2**	**Chan1**	**Chan0**

Bit	Name	Description
15-13, 10–3	Reserved	Reserved—Always write 0 to these bits.
12	ChanType0	Channel Type 0—This bit indicates which type of resource is active for the selected channel. Writing a 1 selects DIFF mode, a 0 selects calibration.
11	AC/DC*	AC/DC Coupling - Writing a 1 to this bit selects AC coupling for the channel, a 0 selects DC coupling. Board powers up with DC coupling enabled.
2–0	Chan<2..0>	Channel Select 2 through 0—These bits indicate which channel is active for the current resource.

Table 3-4. Calibration Channel Assignments

Type<2..0> = CAL			
Chan<3..0>	**PGIA(+)**	**PGIA(-)**	**Purpose**
0000	AOGND*	AOGND*	ADC Offset
0001	AOGND	AIGND	Ground Differential
0010	DAC0OUT	AOGND	DAC 0 Offset/Linearity
0011	DAC1OUT	AOGND	DAC 1 Offset/Linearity
0100	REF5V*	REF5V*	ADC Offset
0001	REF5V	AI GND	ADC Gain
0110	DAC0OUT	REF5V	DAC 0 Gain
0111	DAC1OUT	REF5V	DAC 1 Gain
1xxx	Reserved	Reserved	—

* AIGND on the AT-MIO-16XE-50

Table 3-5. Differential Channel Assignments

Type<2..0> = DIFF		
Chan<3..0>	**PGIA(+)**	**PGIA(-)**
0000	ACh0+	ACH0-
0001	ACh1+	ACh1-
0010	ACh2+	ACh2-
0011	ACh3+	ACh3-
0100	Reserved	Reserved
0001	Reserved	Reserved
0110	Reserved	Reserved
0111	Reserved	Reserved
1xxx	Reserved	Reserved

AI FIFO Offset Load Register

The AI FIFO Offset Load Register sets the depth for the Programmable Empty Flag. This controls when DMA transfers use burst or wait state protocol. This is a strobe register the offset value is set in hardware.

Address: Base address + 3 (hex)
Type: Read-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
7–0	D<7..0>	Data bits 7 through 0— Don't Care

Analog Output Register Group

DAC FIFO Data Register

The DAC FIFO Data Register is used to load the desired data into the DAC data FIFO.

The empty, half-full, and full flags from the DAC data FIFO are available in a status register in the DAQ-STC. These flags indicate when the FIFO is empty, half-full, or full, respectively. Whenever the FIFO is not full the host is free to write additional data.

Address: Base address + 14 (hex)
Type: Write-only
Word Size: 32-bit
Bit Map:

31	***30***	***29***	***28***	***27***	***26***	***25***	***24***
D31	***D30***	***D29***	***D28***	***D27***	***D26***	***D25***	***D24***
23	***22***	***21***	***20***	***19***	***18***	***17***	***16***
D23	***D22***	***D21***	***D20***	***D19***	***D18***	***D17***	***D16***
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	**Name**	**Description**
31–0	D<31..0>	Data bits 31 through 0—The 32-bit data to be written to the DAC data FIFO. This data is interpreted in **straight binary** form.

DAC0 Direct Data Register

The DAC0 Direct Data Register loads the desired data directly into DAC0, without using the DAC data FIFO.

Address: Window address + 00 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	**Name**	**Description**
15–0	D<15:0>	Data bits 15 through 0—The 16-bit data to be written to DAC0, itself. This data is interpreted in **straight binary** form.

DAC1 Direct Data Register

The DAC1 Direct Data Register loads the desired data directly into DAC1, without using the DAC data FIFO.

Address: Window address + 01 (hex)
Type: Write-only

Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15–0	D<15:0>	Data bits 15 through 0—The 16-bit data to be written to DAC1 itself. This data is interpreted in **straight binary** form.

AO FIFO Offset Load Register

The AO FIFO Offset Load Register sets the depth for the Programmable Full Flag. This controls when DMA transfers use burst or wait state protocol. This register must be written after every DAC FIFO clear. The value 0x06 should be written unless a programmable FIFO depth is being used.

Address: Window address + 13 (hex)

Type: Write-only

Word Size: 32-bit

Bit Map:

31	***30***	***29***	***28***	***27***	***26***	***25***	***24***
D31	***D30***	***D29***	***D28***	***D27***	***D26***	***D25***	***D24***

23	***22***	***21***	***20***	***19***	***18***	***17***	***16***
D23	***D22***	***D21***	***D20***	***D19***	***D18***	***D17***	***D16***

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
31–0	D<31..0>	Data bits 31 through 0—These bits set the point at which the programmable full flag is set.

AO Timed Register

The AO Timed register is used to configure each DAC for timed update. The DAC's power on in immediate mode.

Address: Window address + 10 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**DAC1 TIMED**	**DAC0 TIMED**

Bit	**Name**	**Description**
15–2	D<15:2>	Data bits 15 through 2 - Reserved, write 0 at all times
1	DAC1 Timed	DAC1 Timed select - Write a 1 to this bit to configure DAC1 for Timed update. Write a 1 to this bit in the AO Immediate register to configure DAC1 for Immediate Update.
0	DAC0 Timed	DAC0 Timed select - Write a 1 to this bit to configure DAC0 for Timed update. Write a 1 to this bit in the AO Immediate register to configure DAC0 for Immediate Update.

AO Immediate Register

The AO Immediate register is used to configure each DAC for immediate update.

Address: Window address + 11 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**DAC1 Immed**	**DAC0 Immed**

Bit	**Name**	**Description**
15–2	D<15:2>	Data bits 15 through 2 - Reserved, write 0 at all times
1	DAC1 IM	DAC1 Immediate select - Write a 1 to this bit to configure DAC1 for Immediate update. Write a 1 to this bit in the AO Timed register to configure DAC1 for Timed Update.
0	DAC0 IM	DAC0 Immediate select - Write a 1 to this bit to configure DAC0 for Immediate update. Write a 1 to this bit in the AO Timed register to configure DAC0 for Timed Update.

Later Single Point Updates

The Later Single Point Updates register is used configure a DAC so it will receive the timed update pulses at all times. This means the DAC will always receive the Update pulse whether its included in the WG or not. Unlike,

just writing the DAC to the WG Register, in that case after the WG is done and the WG clr register is written those DAC's will no longer receive the update pulse since they have bad points in their buffers.

Address: Window address + 14 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**DAC1 Later Enable**	**DAC0 Later enable**

Bit	**Name**	**Description**
15–2	D<15:2>	Data bits 15 through 2 - Reserved, write 0 at all times
1	DAC1 Later	DAC1 Later select - Write a 1 to this bit to place DAC1 into Later Mode and enable WG. Write a 0 to this bit to remove DAC1 from Later Mode.
0	DAC0 Later	DAC0 Later select - Write a 1 to this bit to place DAC0 into Later Mode and enable WG. Write a 0 to this bit to remove DAC0 from Later Mode.

AO Waveform Generation Register

The AO Waveform generation Register is used to place the DAC into Waveform Generation Mode. This register is used to determine which DACs participate in the WG operation and the order in which they are written. The first DAC written to this register will be the first DAC written during WG.

Address: Window address + 15 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**Dacnum0**

Bit	**Name**	**Description**
15–1	D<15:2>	Data bits 15 through 2 - Reserved, write 0 at all times
0	Dacnum0	DAC0 WG select 0 - This bit controls which DACs participate in WG

Dacnum0	Dac Participating
0	0
1	1

AO Misc Register

The AO Misc Register is used for a variety of AO operations. The WG Clr Strobe bit should be written at the end of a WG operation.

Address: Window address + 16 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**AOPFF INTEN**	**WG CLR STRB**

Bit	Name	Description
15–2	D<15:0>	Data bits 15 through 2 - Reserved, write 0 at all times
1	AOPFF INTEN	AOPFF Interrupt Enable - If this bit is set and interrupt is generated if the AOPFF bit in Status Register is set. Service this interrupt by writing data to the AO FIFO.
0	WG CLR STRB	Waveform Generation Clear Strobe - Write a 1 to this bit to clear all DACs from waveform generation (unless in later single point mode). This bit should always be written at the conclusion of a WG operation.

DMA Control Register Group

AI AO Select Register

The AI AO Select Register select the DMA channel used for Analog Output and Analog Input. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 09 (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
AO CHD	**AO CHC**	**AO CHB**	**AO CHA**	**AI CHD**	**AI CHC**	**AI CHB**	**AI CHA**

Bit	Name	Description
7–4	AO CH<D..A>	Analog Output DMA Channel D through A—These bits select the DMA channels to be used by analog output. These bits must be set prior to enabling the channel.
3–0	AI CH <D..A>	Analog Input DMA Channel D through A—These bits select the DMA channel to be used by analog input. These bits must be set prior to enabling the channel.

G0 G1 Select Register

The G0 G1 Select Register select the DMA channel used by the General Purpose Counters. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 0B (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
GP1 CHD	**GP1 CHC**	**GP1 CHB**	**GP1 CHA**	**GP0 CHD**	**GP0 CHC**	**GP0 CHB**	**GP0 CHA**

Bit	**Name**	**Description**
7–4	GP1 CH <D..A>	General Purpose Counter Timer 1 DMA Channel D through A—These bits select the DMA channel that the GPCT1 uses. These bits must be set prior to enabling the DMA channel.
3–0	GP0 CH <D..A>	General Purpose Counter Timer 0 DMA Channel D through A—These bits select the DMA channel that the GPCT1 uses. These bits must be set prior to enabling the logical channels.