

**Technical Reference Manual
for AD PP5/002 CompactPCI®
Bus Transition Module**

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CONVENTIONS

Throughout this manual the following conventions will apply:

- # or * after a name represents an active low signal. e.g. INIT* or INIT#
- h denotes a hexadecimal number. e.g. FF45h
- byte represents 8-bits
- word represents 16-bits
- dword represents 32-bits

NOTATIONAL CONVENTIONS

NOTE: Notes provide general additional information.

WARNING: Warnings provide indication of board malfunction if they are not observed.

CAUTION: Cautions provide indications of board or system damage if they are not observed

GLOSSARY OF TERMS

ATA	AT Attachment
CODEC	Coder / Decoder
DFP	Digital Flat Panel
DIL	Dual In-Line
DVI	Digital Video Interface
EIDE	Enhanced Integrated Drive Electronics
ETH.....	Ethernet
GND	Ground (Power and Signal Common Reference (0V))
IDC.....	Insulation Displacement Connector
I/O	Input Output
KBD	Keyboard
LCD.....	Liquid Crystal Display
LED	Light Emitting Diode
LVD	Low Voltage Differential
MDR.....	Mini-D Ribbon
NC.....	Not Connected
PC-AT	Personal Computer-Advanced Technology
SATA	Serial AT Attachment
SCSI	Small Computer Systems Interface
SPKR.....	Speaker
TM.....	Transition Module
USB	Universal Serial Bus
VCC	Voltage Collector Current
VGA	Video Graphics Array

REVISION HISTORY

Revision	Summary of Changes	Date
01	First Release	August 2006
02	Updated for Rev B and Rev C boards	January 2007

NOTE: Switch block SW5 has changed orientation on the Rev B and Rev C boards from its position on the Rev A version. Section 2.3 contains a complete layout showing all switch positions.

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1 INTRODUCTION

1.1 General

The AD PP5/002 Transition Module is designed primarily to complement the Concurrent Technologies CompactPCI PP 41x/03x processor boards. It provides the rear panel I/O interface connectors for the following interfaces: SATA x 2, PMC I/O (or SCSI) x 2, serial port, 10/100/1000Mbps Ethernet ports, USB ports and stereo audio line level interface.

The AD PP5/002 Transition Module conforms to the IEEE P1101.11 & 1101.10 form factors as specified in the CompactPCI specification. It requires 1 rear panel slot (4HP).

Figure 1-1 is a block diagram of the Transition Module showing the main connections provided by the board. Further details are given in Chapter 3 and Appendix A.

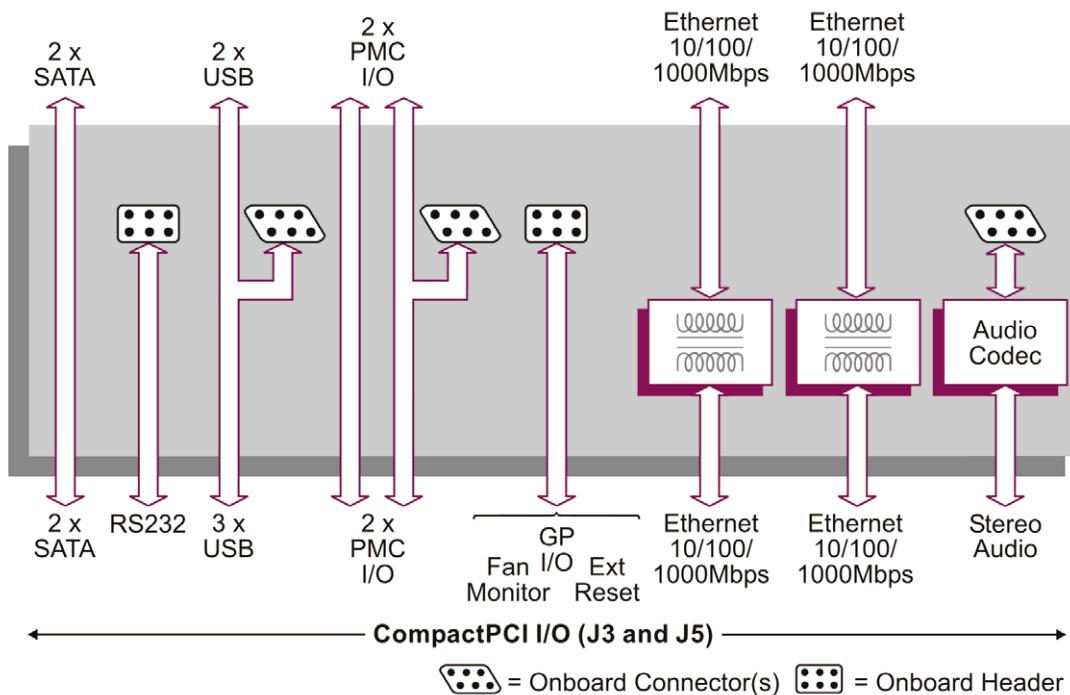


Figure 1-1 Overview

INTRODUCTION

1.2 Compliance to RoHS 2002/95/EC

This product is offered in a form which complies to the RoHS 2002/95/EC directive. The European Union RoHS 2002/95/EC directive restricts the use of six materials in electronic components and assemblies. Specifically, these materials are Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr VI), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE). Concurrent Technologies is committed to compliance to the RoHS directive.



The product may also be available in an alternative form which includes components which do not comply with the RoHS directive. Consult your supplier to determine order codes for RoHS compliant and non-compliant products.

2 INSTALLATION

2.1 General

This chapter contains general information on unpacking and inspecting the AD PP5/002 after shipment, installation and powering up the board.

CAUTION: It is strongly advised that, when handling the AD PP5/002 and its associated components, the user should at all times wear an earthing strap to prevent damage to the board as a result of electrostatic discharge.

2.2 Unpacking and Inspection

Immediately after the board is delivered to the user's premises the user should carry out a thorough inspection of the package for any damage caused by negligent handling in transit.

CAUTION: If the packaging is badly damaged or water-stained the user must insist on the carrier's agent being present when the board is unpacked.

Once unpacked, the board should be inspected carefully for physical damage, loose components etc. In the event of the board arriving at the customer's premises in an obviously damaged condition Concurrent Technologies or its authorized agent should be notified immediately.

INSTALLATION

2.3 Factory Settings

The AD PP5/002 is fitted with several switches to configure some of the interfaces. Board functionality is not described here in detail. It is recommended that any user unfamiliar with the AD PP5/002 should read Chapter 3, Functional Description, before attempting to alter the existing board configuration.

Figure 2-1 shows the default switch positions for Rev B and Rev C boards. Figure 2-2 shows the default positions for Rev A boards only. Rev A boards may be identified by their different rectangular shape, but the revision number is also printed on the top side of the board.

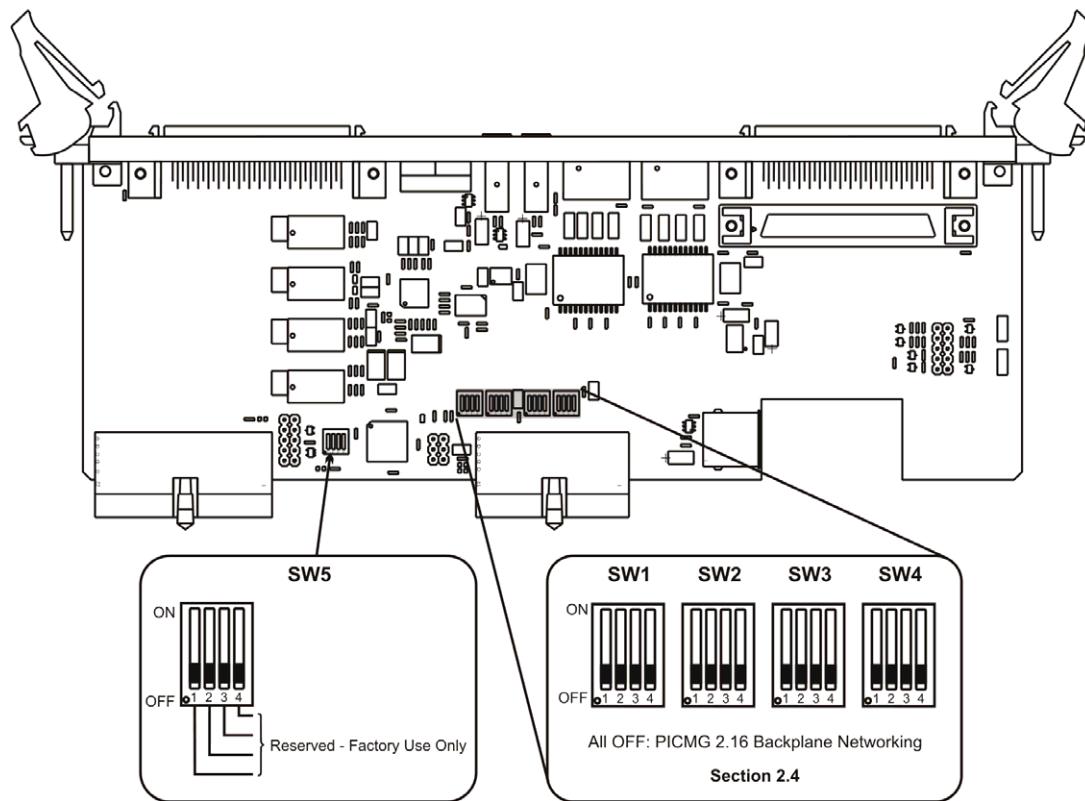


Figure 2-1 Factory Switch Settings (Rev B and Rev C boards)

NOTE: Switch block SW5 has changed orientation on the Rev B and Rev C boards from its position on the Rev A version. All switches on this block should remain in the OFF position.

INSTALLATION

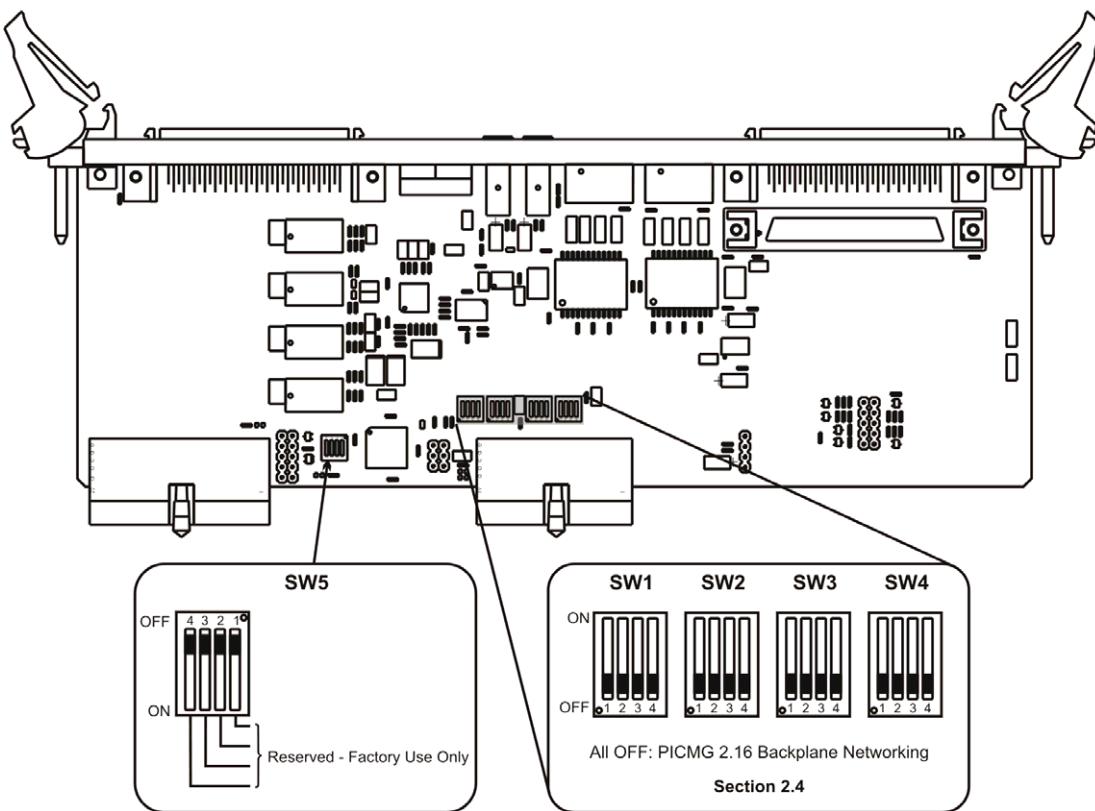


Figure 2-2 Factory Switch Settings (Rev A boards)

INSTALLATION

2.4 Ethernet DIL Switches

The AD PP5/002 is designed to operate with companion processor boards which may be configured either to have rear panel Ethernet connections via P3/J3, or to have PICMG 2.16 connections via P3/J3. If the processor board is configured for PICMG 2.16 connections, the backplane pins must be isolated from the Ethernet interfaces on the AD PP5/002. Switches are provided to allow this isolation to be performed either by the user or at the factory, and are shown in Figure 2-2 below.

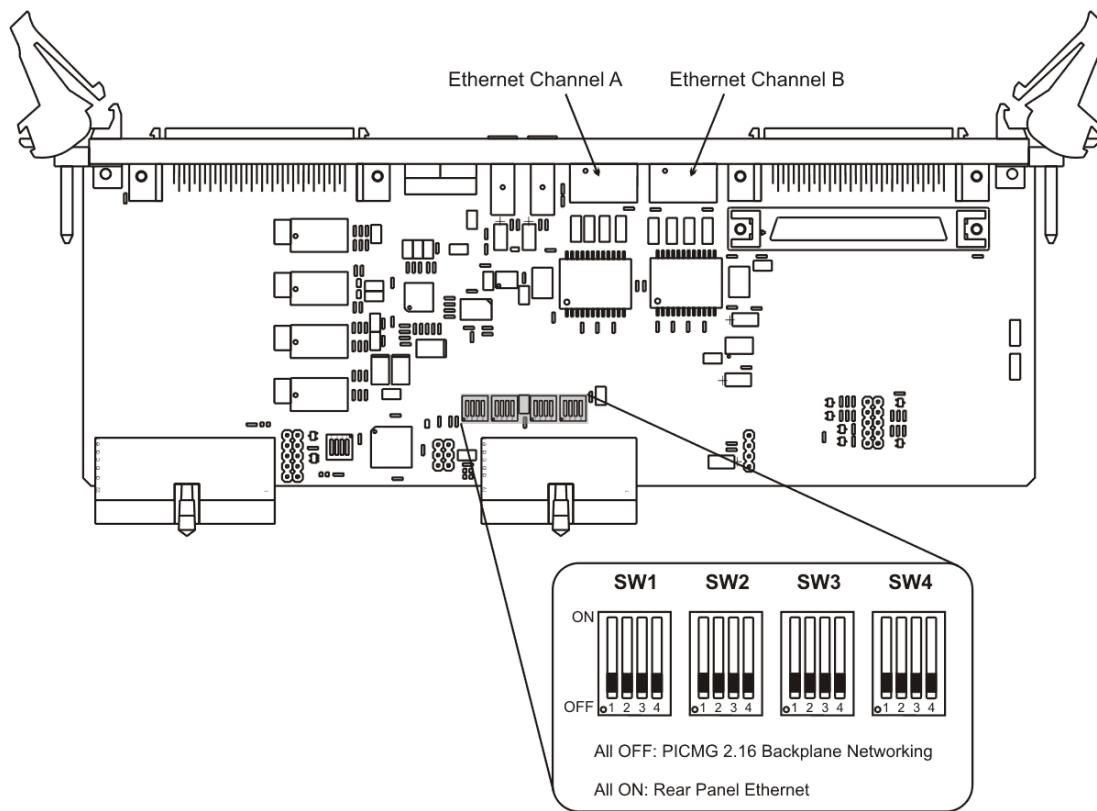


Figure 2-3 Ethernet DIL Switches

SW1 and SW2 configure Ethernet channel A.

SW3 and SW4 configure Ethernet channel B.

INSTALLATION

2.5 Installation and Power-up

Once the AD PP5/002 has been configured to the user's requirements (see Chapter 3) it can be installed in the system backplane.

The board is installed and powered up as follows:

- 1) Make sure that system power is turned OFF (see note below regarding Hot Swap installation or removal).
- 2) Slide the board into the designated slot, making sure that the board fits neatly into the runners.
- 3) Push the board into the card-cage until the J3 - J5 connectors are firmly located. Use the injector/ejector handle for the final push.
- 4) Screw the ejector handle retaining bolt into the hole in the chassis.
- 5) Connect up the I/O cables to the connectors on the board's front panel and fix in place with the connectors' retaining screws.
- 6) Power-up the system.

NOTE: It may be more convenient to attach cables to the onboard connectors before inserting the board into the card-cage (Step 3).

INSTALLATION

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3 FUNCTIONAL DESCRIPTION

3.1 General

In order to fully understand the operations of the AD PP5/002 board, the user may wish to understand some of the details of the board hardware. This chapter offers some further details for each of the functional areas of the board.

3.2 Functional Description

Figure 3-1 shows a functional overview of the AD PP5/002. The following sections give details of each functional block. Connector types, locations and pin-outs are detailed in Appendix A.

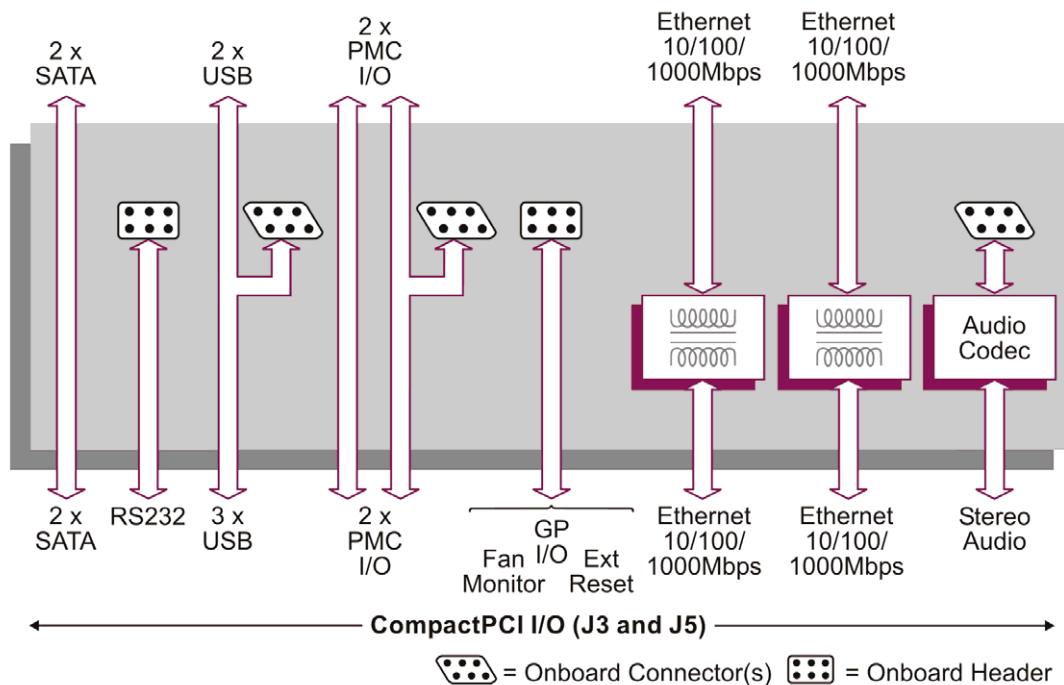


Figure 3-1 Overview

FUNCTIONAL DESCRIPTION

3.3 USB

The USB1 (P1) and USB2 (P2) interfaces are provided on the AD PP5/002 front panel; USB3 is provided either using an in-board right-angle USB connector (P3, Rev B onwards) or an in-board 4-pin header (LK2, Rev A only).

3.4 Ethernet

Ethernet channels A and B on J3 are provided on two RJ45 connectors on the AD PP5/002 front panel.

The connectors have two LED indicators. The yellow LED flashes when the interface is operating at 1000Mbits/s; lights constantly when the interface is operating at 100Mbits/s and is off when the interface is operating at 10Mbits/s. The green LED lights when a link is established and flashes during data transmission. The LEDs are controlled by a multiplexed I/O signaling system which uses pins on the J5 backplane connector.

NOTE: In order to use these interfaces, all poles of the Ethernet DIL switches must be ON.

3.5 SATA Interfaces

The two Serial ATA interfaces on J5 are routed to a dual SATA connector on the front panel (S1).

3.6 PMC I/O

The I/O signals from the companion processor board PMC Site 1 appear on J5 and are routed to a 68-way female high-density D connector (J6) on the AD PP5/002 front panel. The pin-out and wiring is compatible with Concurrent Technologies SCSI PMC modules.

The I/O signals from the companion processor board PMC Site 2 appear on J3 and are routed to two 68-way female high-density D connectors. One of these connectors (J9) is mounted on the AD PP5/002 front panel, the other (J10) is located just inside the front panel. The pin-out and wiring of both connectors is identical and is compatible with Concurrent Technologies SCSI PMC modules.

3.7 Stereo Audio

The AD PP5/002 supports stereo audio line-in and line-out interfaces, together with a stereo headphone output and mono microphone input. These interfaces are derived from an AC'97 audio connection through the CompactPCI J3 connector, using an audio CODEC fitted to the AD PP5/002. The interfaces are accessible via 3.5mm stereo jack sockets mounted horizontally in-board (J11-J14). The line-in inputs will accept 2V_{rms} input voltages.

The legacy PC speaker output signal (on J3 pin A1) is fed into the audio CODEC. This allows the speaker tones to be heard on the line and headphone outputs.

3.8 RS232 Serial Port

An RS232 serial port interface is provided using a 10-pin header (LK4) mounted in-board. This interface is connected to the companion processor board via the CompactPCI J3 connector.

3.9 General Purpose I/O

Two TTL compatible General Purpose output signals are provided. These outputs may be set or reset by writing to the General Purpose I/O register(s) on the companion processor board.

Two TTL compatible General Purpose input signals are provided. The state of these inputs may be read in the General Purpose I/O register(s) on the companion processor board.

A SPECIFICATIONS

A.1 Functional Specification

PMC I/O:	<ul style="list-style-type: none">• 64 I/O signals from each site routed to rear panel high-density D-type sockets.• PMC site 2 I/O also routed to on-board vertically mounted high-density D-type socket.
Network:	<ul style="list-style-type: none">• RJ45 connectors on rear panel supporting 10/100/1000Mbits/s Ethernet from CompactPCI J3 backplane connector.• Isolation switches provided for use with companion processor boards configured for PICMG 2.16 interface.
Mass Storage:	<ul style="list-style-type: none">• Two SATA-150 rear panel connectors.
Serial Comms:	<ul style="list-style-type: none">• One 10-pin header for RS232 COM port on companion processor board.• Two USB ports on rear panel.• One USB port via in-board connector or 4-pin header.• Stereo audio line-level connections for Line In, Line Out, Headphones Out, Microphone In, using horizontal in-board jack sockets.• General Purpose I/O and Fan Sensor inputs on 10-pin header; signals provided by companion processor board via multiplexed I/O interface.

SPECIFICATIONS

A.2 Environmental Specification

A.2.1 Temperature Range

Operating	0 to +55 degrees Celsius
Storage	-40 to +85 degrees Celsius

A.2.2 Humidity

Operating	10% to 90% non-condensing
Storage	10% to 90% non-condensing

SPECIFICATIONS

A.3 Dimensions

Height	13.5mm
Depth	80mm
Width	233mm
Weight	270 g

SPECIFICATIONS

A.4 Electrical Specification

A.4.1 Power Supply Requirements

VOLTAGE (V)	REGULATION	CURRENT (typical)
+5.0V	+/-5%	0.2A
+3.3V	+/-5%	0.1A

Table A-1 Power Supply Requirements

NOTE: With no interface drawing power. Interfaces that draw power e.g. USB, will add to the +5.0V current.

SPECIFICATIONS

A.5 Connectors

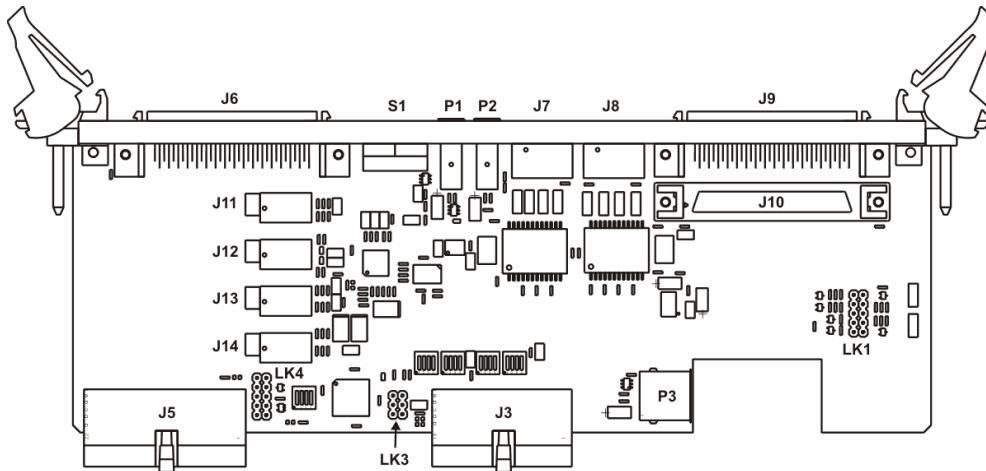


Figure A-1 Connector Layout (Rev B and Rev C boards)

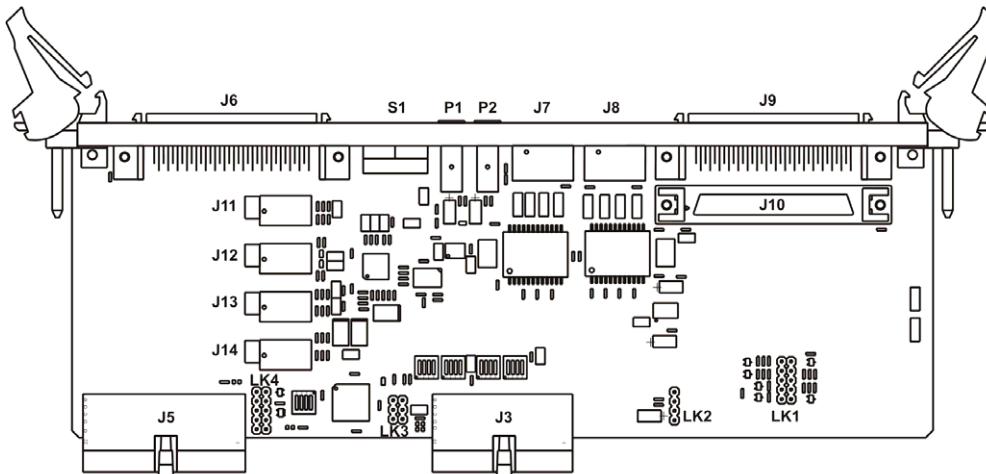


Figure A-2 Connector Layout (Rev A boards)

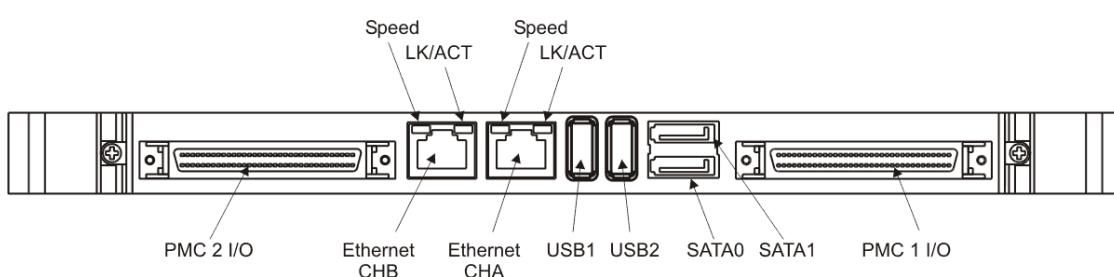


Figure A-3 Front Panel Connector Layout

SPECIFICATIONS

A.5.1 CompactPCI Interface (J3) Pin-outs

The CompactPCI interface I/O connector J3 consists of a 114-way connector with pins assigned as follows:

Pin	A	B	C	D	E	F	
19	GND	GND	GND	GND	GND	GND	Ethernet
18	LPa_DA	LPa_DA#	GND	LPa_DC	LPa_DC#	GND	
17	LPa_DB	LPa_DB#	GND	LPa_DD	LPa_DD#	GND	
16	LPb_DA	LPb_DA#	GND	LPb_DC	LPb_DC#	GND	
15	LPb_DB	LPb_DB#	GND	LPb_DD	LPb_DD#	GND	
14	+3.3V	+3.3V	TMSENSE	+5V	+5V	GND	
13	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	GND	
12	I/O 10	I/O 9	I/O 8	I/O 7	I/O 6	GND	
11	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	GND	
10	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16	GND	
9	I/O 25	I/O 24	I/O 23	I/O 22	I/O 21	GND	
8	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	GND	PMC 2 I/O
7	I/O 35	I/O 34	I/O 33	I/O 32	I/O 31	GND	
6	I/O 40	I/O 39	I/O 38	I/O 37	I/O 36	GND	
5	I/O 45	I/O 44	I/O 43	I/O 42	I/O 41	GND	
4	I/O 50	I/O 49	I/O 48	I/O 47	I/O 46	GND	
3	I/O 55	I/O 54	I/O 53	I/O 52	I/O 51	GND	
2	I/O 60	I/O 59	I/O 58	I/O 57	I/O 56	GND	
1	SPKR Out	I/O 64	I/O 63	I/O 62	I/O 61	GND	
Pin	A	B	C	D	E	F	

Table A-2

CompactPCI J3 Interface Pin-outs

SPECIFICATIONS

A.5.2 CompactPCI Interface (J5) Pin-outs

The CompactPCI interface I/O connector J5 consists of a 132-pin connector with pins assigned as follows:

Pin	A	B	C	D	E	F	
22	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	GND	
21	I/O 10	I/O 9	I/O 8	I/O 7	I/O 6	GND	
20	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	GND	
19	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16	GND	
18	I/O 25	I/O 24	I/O 23	I/O 22	I/O 21	GND	
17	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	GND	
16	I/O 35	I/O 34	I/O 33	I/O 32	I/O 31	GND	
15	I/O 40	I/O 39	I/O 38	I/O 37	I/O 36	GND	
14	I/O 45	I/O 44	I/O 43	I/O 42	I/O 41	GND	
13	I/O 50	I/O 49	I/O 48	I/O 47	I/O 46	GND	
12	I/O 55	I/O 54	I/O 53	I/O 52	I/O 51	GND	
11	I/O 60	I/O 59	I/O 58	I/O 57	I/O 56	GND	
10	GND	I/O 64	I/O 63	I/O 62	I/O 61	GND	
9	TM_RST#	GND	GND	GND	GND	GND	
8	SATA0R	SATA0R#	GND	SATA0T	SATA0T#	GND	SATA0
7	SATA1R	SATA1R#	GND	SATA1T	SATA1T#	GND	SATA1
6	GND	GND	AC_BITCLK	COMDSR	COMDTR	GND	
5	USBD2#	USBD2	AC_SDIN	COMCTS	COMRTS	GND	
4	USBD3#	USBD3	AC_SDOUT	COMRXD	COMTXD	GND	
3	LDRQ1#	MUXIO_DATA	MUXIO_CLK	RFU	COMDCD	GND	MUXIO,
2	LAD3	LAD2	LAD1	LAD0	GND	GND	LPC &
1	USBD1#	USBD1	SERIRQ	LFRAME#	TM_CLK	GND	USB1
Pin	A	B	C	D	E	F	

Table A-3

CompactPCI J5 Interface Pin-outs

SPECIFICATIONS

A.5.3 USB1 (P2), USB2 (P1) and USB3 (P3 / LK2) Connectors

Two of the three USB ports available on the AD PP5/002 are interfaced through standard USB sockets on the front panel. The third port is interfaced either through an in-board right-angle USB connector (P3) or a 4-way pin header (LK2) located close to the backplane edge of the board (see Figures A-1 and A-2). Figure A-3 and Tables A-4 through A-6 show the locations of the front panel and the pinouts of all the USB connectors.

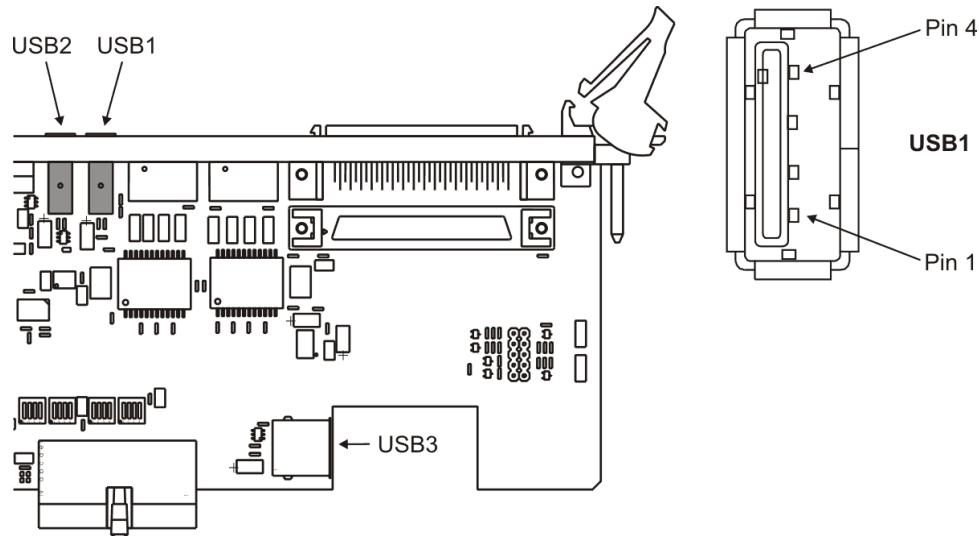


Figure A-4 USB1 (P2) and USB2 (P1) Connectors

Pin	Signal Name
1	USB VCC (+5V)
2	USBD -
3	USBD+
4	USB GND

Table A-4 USB1 (P2) and USB2 (P1) Connector Pin-outs

Pin	Signal Name
1	USB VCC (+5V)
2	USBD -
3	USBD+
4	USB GND

Table A-5 USB3 (P3 on Rev B and Rev C boards) Connector Pin-outs

Pin	Signal Name
4	USB GND
3	USBD+
2	USBD -
1	USB VCC (+5V)

Table A-6 USB3 (LK2 on Rev A boards) Connector Pin-outs

NOTE: USB VCC is protected by a 750mA self resetting current limiting device (one per interface).

SPECIFICATIONS

A.5.4 Ethernet RJ45 Channel A (J7) and Channel B (J8) Connectors

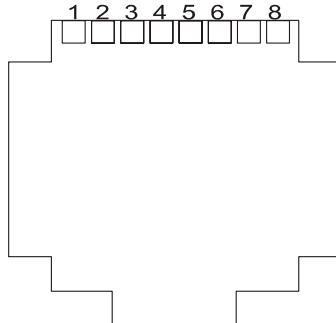


Figure A-5 **Ethernet RJ45 Connector (Front View)**

Pin	10/100 Signal Name	1000 Signal Name
1	Transmit (+)	LPx_DA
2	Transmit (-)	LPx_DA#
3	Receive (+)	LPx_DB
4	Not used	LPx_DC
5	Not used	LPx_DC#
6	Receive (-)	LPx_DB#
7	Not used	LPx_DD
8	Not used	LPx_DD#

Table A-7 **Ethernet (J7 and J8) RJ45 Connector Pin-outs**

Yellow LED = Connection speed.

- Flashing = 1000Mbits/s.
- On = 100Mbits/s.
- Off = 10Mbits/s.

Green LED = LINK/ACTIVITY indicator:

- Flashing = Activity.
- On = Connected.
- Off = Not Connected.

SPECIFICATIONS

A.5.5 Serial Interface (LK4) Connector

The location of the Serial Interface connector is shown in Figure A-6 and the pinout is detailed in Table A-8.

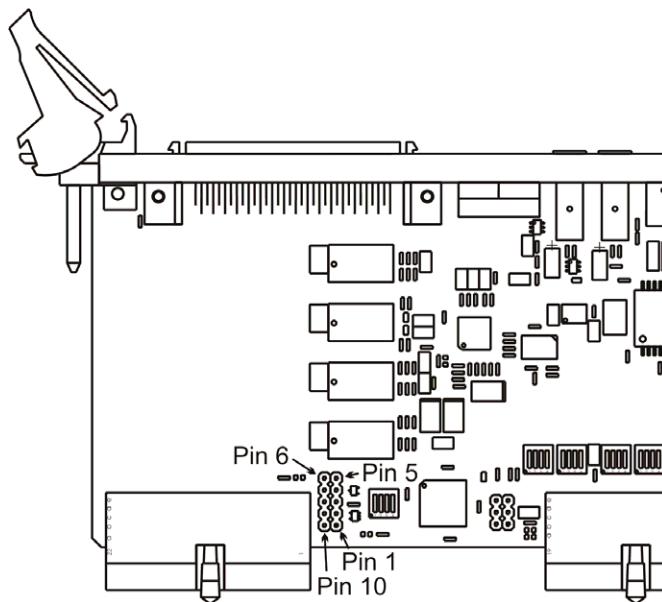


Figure A-6 **Serial Interface (LK4) Header**

Pin No.	Signal Name	Pin No.	Signal Name
6	NC	5	GND
7	RI - Ring Indicator	4	DTR – Data Terminal Ready
8	CTS – Clear to Send	3	TXD# – Tx Data
9	RTS – Request to Send	2	RXD# – Rx Data
10	DSR – Data Set Ready	1	DCD – Carrier Detect

Table A-8 **Serial Port (LK4) Header Pin-outs**

The standard PC-AT serial port connector is a 9-way Male Sub-miniature D-type. The correspondence between the AD PP5/002 10-pin header pin-out, the ribbon cable cores and the PC-AT 9-pin D-type serial connector pin-out is defined in the table below.

Signal Name	Header Pin	Ribbon Cable Core	PC-AT Pin
DCD	1	1	1
DSR	10	2	6
RXD#	2	3	2
RTS	9	4	7
TXD#	3	5	3
CTS	8	6	8
DTR	4	7	4
RI	7	8	9
GND	5	9	5

Table A-9 **Serial Port Cable Connections**

NOTE: The pinout on LK4 has been chosen to give the correct PC-AT serial port pinout with a ribbon cable connection to a 9-way male D-type connector. This assumes that pin 1 of LK4 connects to pin 1 of the D-type connector.

SPECIFICATIONS

A.5.6 General Purpose I/O (LK1) Connector

The General Purpose I/O signals are made available on a 10-pin header. The GP Output lines are TTL compatible. They have 100 Ohm series current limiting resistors and over/under voltage protection diodes. They can sink or source up to 10mA.

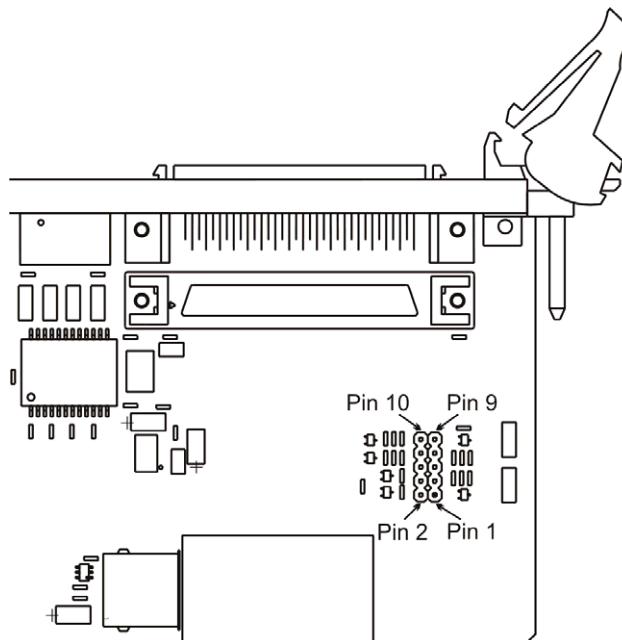


Figure A-7 General Purpose I/O (LK1) Header (Rev B and Rev C boards)

NOTE: For the location of LK1 on Rev A boards, please refer to Figure A-2.

Connect pins 1 and 3 to reset the companion processor board. Connect the fan sensor to pins 5 and 7. Pin 5 is the (open collector) sense signal. Pin 7 is GND. The GP Input lines are TTL compatible. All four inputs have 10K pullups to +5V and under/over voltage protection diodes.

Pin No.	Signal Name	Direction	Pin No.	Signal Name	Direction
10	GP Input 1	Input	9	VCC (+5V)	
8	GP Input 0	Input	7	GND	
6	GP Output 1	Output	5	Fan Sensor	Input
4	GP Output 0	Output	3	Ext Reset	Input
2	GND		1	GND	

Table A-10 General Purpose I/O (LK1) Header Pin-outs

SPECIFICATIONS

A.5.7 PMC I/O Connectors (J6, J9 and J10)

The PMC I/O signals are made available on three 68-way High Density D-Type connectors. The signals from companion processor board PMC site 1 appear on J6 and the signals from the companion processor board PMC site 2 appear on J9 and J10. The pin-out for these connectors is shown in Table A-11 below.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	I/O 1	18	NC	35	I/O 2	52	I/O NC
2	I/O 3	19	NC	36	I/O 4	53	I/O NC
3	I/O 5	20	I/O 35	37	I/O 6	54	I/O 36
4	I/O 7	21	I/O 37	38	I/O 8	55	I/O 38
5	I/O 9	22	I/O 39	39	I/O 10	56	I/O 40
6	I/O 11	23	I/O 41	40	I/O 12	57	I/O 42
7	I/O 13	24	I/O 43	41	I/O 14	58	I/O 44
8	I/O 15	25	I/O 45	42	I/O 16	59	I/O 46
9	I/O 17	26	I/O 47	43	I/O 18	60	I/O 48
10	I/O 19	27	I/O 49	44	I/O 20	61	I/O 50
11	I/O 21	28	I/O 51	45	I/O 22	62	I/O 52
12	I/O 23	29	I/O 53	46	I/O 24	63	I/O 54
13	I/O 25	30	I/O 55	47	I/O 26	64	I/O 56
14	I/O 27	31	I/O 57	48	I/O 28	65	I/O 58
15	I/O 29	32	I/O 59	49	I/O 30	66	I/O 60
16	I/O 31	33	I/O 61	50	I/O 32	67	I/O 62
17	I/O 33	34	I/O 63	51	I/O 34	68	I/O 64

Table A-11 PMC I/O (J6, J9 and J10) Connector Pin-outs

The connectors used on the rear panel (J6 and J9) are one of the following types:

- Molex 15-87-6024 or AMP 1761028-4

Screwlocks for this connector are also supplied with the board but are not fitted.

The connector used on the board (J10) is of the following type:

- AMP 5749069-7

No screwlocks are supplied for this connector.

SPECIFICATIONS

A.5.8 SATA (S1) connectors

The pin-out for the SATA Interface connectors is shown in Table A-12.

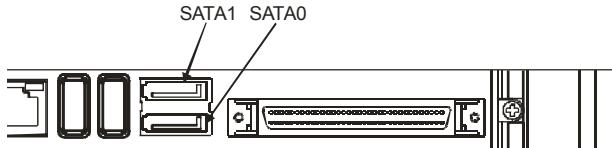


Figure A-8 **SATA (S1) Connectors**

Pin No.	Signal
1	GND (0V)
2	SATA 0/1 Tx+
3	SATA 0/1 Tx-
4	GND (0V)
5	SATA 0/1 Rx-
6	SATA 0/1 Rx+
7	GND (0V)

Table A-12 **SATA (S1) Connector Pin-outs**

SPECIFICATIONS

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