ALPHA DATA
BEAM

CERN Trajectory Measurement System

Project Status

Project	CERN-TMS
Date	2007-06-28
Reference	Cern-tms/status-5
Author	Terry Barnaby

1. Overview

The two pre-series systems have been on test at Alpha Data and CERN. Further software and FPGA development has also been carried out.

2. Work Done

The following work has been performed:

- A full characterisation test on the PUPE ADC's has been performed by Alpha Data. There is a some noise in the ADC output. The source of this has been found to be mainly due to a tracking issue with the 5V power supply to the FPGA, causing switching regulator noise to be injected into the ADC analogue signals. A small PCB layout change will reduce this noise significantly. This change is under way.
- The ADC clock PLL has been synchronised with the 10MHz system clock. Some minor changes around the PLL will improve the lock stability. These changes are being carried out.
- A number of minor PUPE board issues have been noted and modifications will be carried out in the next board revision.
- The ADC firmware has been modified to build with the Xilinx XST tool. This will make it easier to CERN to further develop the FPGA firmware.
- The issues with writing to some registers on the PUPE board has been fixed.
- The ADC data latch time in the FPGA has been changed to match the ADC data timings.
- The problem with loading the FPGA internal test data from SDRAM system has been fixed.
- The TmsControlGui test application has been improved with abilities to setup and edit the State/Phase tables.
- The TmsControlGui test application has been improved to store data files in user defined locations.
- Testing of the full pre-series system has been carried out and a number of FPGA firmware and Software changes have been made.
- The source code for the TMS API has been sent to CERN's system software staff to allow them to port this to their LynxOS based platform.
- CERN have been performing tests on the pre-series system. They have also noticed the 30 to 45MHz noise hump due to switching regulator noise injection.

3. Work Todo

A decision on any changes to the PUPE board design needs to be made shortly. Some of the changes to be made and some possibilities are listed below:

1. A PCB layout improvement to the FPGA 5Volt signal path will be made to reduce ADC noise.
2. Some changes around the ADC clock PLL will be made to improve its lock stability.
3. The ADC harmonic distortion figures need to be looked at. There are some ADC resistor values that could be tweaked to reduce the harmonic distortion.
4. A decision is needed as to the ADC voltage input range. It is currently +-2 Volts (4 Volts p-p). It could be set to +-1 Volt (2 Volts p-p). Setting the input range to +-1 Volt would increase the level of noise pickup in the cabling and reduce the ADC input over voltage protection.
5. A decision is needed on the TTL digital timing signal termination impedance. This is currently 50 ohms. We could increase this to 100 ohms or perhaps higher to reduce the power levels needed to drive these lines and the power dissipation on the PUPE board.

FPGA Firmware and Software changes

1. The Software will be further developed for full system implementation. Data transfer performance and error handling will be investigated and modified as required.
2. The FPGA firmware will be further developed as required based on pre-series testing.

4. Current Schedule

The pre-series system was delivered slightly behind the original schedule. The detailed project schedule is at: https://portal.beam.ltd.uk/support/cern/schedule.php.

We have agreed with CERN a new full system delivery date that is a little behind the original contract date. This will allow us and CERN to perform more testing with the pre-series system and implement improvement to the system prior to full system delivery. We do need a quick agreement to the full system production from CERN in order to meet these time-scales.

The basic schedule information is:

Item	Date	Original Date
PUPE PCB redesign start	July 2nd	
CERN Agrees to full system production	July 6th	May 11th
Order main board components (FPGAS)	July 9th	
PUPE PCB redesigned	July 30th	
PUPE board manufacture starts	August 20th	
TMS full system testing	September 3rd	
Full System Installation	October 2nd	August 21st