

Project	CERN-TMS
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1. Overview

The second production run of the PUPE boards was completed and the boards have had basic functional testing performed. The TMS pre-series system has been assembled and basic testing with the TMS test signal generator has been performed. We have installed and performed basic testing with the TMS system on the actual PS machine at CERN as part of the pre-series installation visit.

2. Work Done

The following work has been performed:

- The second production run of the PUPE boards has been completed.
- The PUPE boards have been functionally tested to a basic level. Full testing and ADC characterisation tests have yet to be performed. There may be a production issue with the cPCI termination resistor packs.
- The FPGA firmware has been ported to the PUPE board and has been tested with the full TMS system software using the TMS test signal generator. There are a few minor issues to be resolved.
- The TMS software has been tested and further developed using the PUPE board, FPGA Firmware and TMS test signal generator.

3. CERN Pre-Series Visit

We visited CERN on the 6/6/2007 through to 8/6/2007 to install the TMS pre-series system and perform initial testing with the CERN PS machine. The work done during this visit included:

- The system was set-up and tested stand-alone with the TMS test signal generator to make sure all components were OK after transportation to CERN. All parts functioned fine.
- With CERN's help, we installed the TMS rack components into one of CERN's main racks and again performed tests with the TMS test signal generator to make sure all components were OK. There was a problem at this stage due to a loose bolt finding its way into the power supply causing a warning light to be on. We have brought this power supply back for testing.
- We then demonstrated the TMS system's software to CERN's staff and showed the system working with the TMS test signal generator.
- The system was then connected to the CERN PS machine using the CYCLE_START, FREF, INJECTION and Sigma signals. The 10MHz SYS_CLOCK was provided by the TMS test signal generator and the CYCLE_STOP signal was supplied by software. Once the pllInitialFrequency and frefPhaseDelay0 was setup to match the PS machine the TMS PLL was seen to lock and the system was seen to capture data.
- It was noticed that the PLL took some time to lock. One reason for this was that the PLL was

running at 62.5MHz rather than 125MHz as per CERN's original example code. Andrew updated the firmware for this and we later worked with the 125MHz PLL.

- It was noticed that the ADC data had some glitches on the DeltaX and DeltaY inputs. Derek had a look at this and Andrew modified the firmware to latch the ADC data on the opposite clock edge to fix this issue. This needs further investigation.
- It was noticed that the final data from the system looks a little noisy. This needs some further investigation. The actual analogue input signals were quite low. It may be better to set the TMS system to use +-1 Volt peak-peak input signals rather than the current +-2 Volt peak-peak setting.
- Derek worked on the ADC PLL clock synchronisation chip during the visit as well as looked at the ADC data latch timing issue..
- We helped CERN get the TMS system running on their network and accessible from their remote computers.
- We gave basic training to CERN's staff on how to use and test the system.
- We had a meeting with some of CERN's software support staff to help them with integrating the system into the CERN main control systems.

The pre-series visit and installation went very well. We were able to connect the system to the CERN PS and capture and process live signals from the system. The diagnostics and test systems worked well. There are a few issues too investigate and fix.

4. Work Todo

- A full characterisation test on the PUPE ADC's needs to be performed. Alpha Data and CERN will carry out this work. This is probably best done using Derek's ADC test FPGA code.
- We need to look at the noise in the final data to see where this is coming from. This could be ADC capture noise or a problem in the FPGA algorithm possibly the BLR algorithm.
- The ADC clock's PLL needs the option to be able to be synchronised with the 10MHz system clock. We need to setup the PLL chip and test this functionality.
- There are some issues with writing to some registers on the PUPE board. This is causing the pllPhaseDelay register to not be set occasionally and the diagnostics capture to occasionally fail.
- We need to check the ADC data latch time in the FPGA to make sure it is in phase with the ADC data.
- There is some problem where the FPGA bit file will not run after the first load from a cold boot.
- There is some problem with the FPGA internal test data from SDRAM system in the current firmware release.
- The TmsControlGui test application could be improved to add abilities to setup the State/Phase tables.
- The TmsControlGui test application could be improved to store data files in user defined locations.
- We will provide the source code for the TMS API to CERN's system software staff and assist them in porting this to their LynxOS based platform.
- Full series system work including testing with multiple PUPE boards, Module Controllers and client

applications.

5. Parts Delivered

The following TMS hardware has been delivered to CERN:

- 1 x cPCI Full Rack.
- 1 x Compact PCI Module controller.
- 1 x Network Switch.
- 1 x System Controller.
- 1 x PUPE board
- 1 x PUPE timing panel.

6. Current Schedule

The pre-series system was delivered slightly behind the original schedule. The detailed project schedule is at: <https://portal.beam.ltd.uk/support/cern/schedule.php>.

Although we are a little behind with shipping the pre-series system we can deliver the full system on time assuming we get an early agreement to full system production from CERN. However, we believe it would be much better for both parties to spend more time with the pre-series system performing testing prior to agreeing to the final system production. This we believe would yield a better system for CERN. We understand that there are no real project pressures for the August 21st date. The main project pressure is to have a functioning system prior to the end of year PS shutdown leaving sufficient time for CERN to test the system on real BEAM signals this year. A date of the 28th of September was thought to be mutually acceptable. We need to confirm this.

The basic schedule information is:

Item	Date	Original Date
Pre-Series Unit Complete	May 29 th	May 4th
Pre-series installation	June 6th	
CERN Agrees to full system production	June 20th	May 11th
Full System Installation	September 28 th ?	August 21st