ALPHA DATA
BEAM

CERN Trajectory Measurement System

Initial Project Meeting

Project	CERN-TMS
Date	2006-10-16
Reference	Cern-tms/meeting-1
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1. References

- IT-3384/AB: Technical Specification for a new trajectory measurement system for the CERN Proton Synchrotron.
- Alpha Data's CERN Trajectory Measurement System "pre-design-1.5"

2. Introduction

Staff from Alpha Data and Beam Ltd had a meeting on the 16th of October 2006 to discuss the CERN Trajectory Measurement System project. The meeting covered all aspects of the system design and project schedules.

3. System Design

A number of possible system improvements to the system's design as given in the "pre-design-1.5" document were discussed. These were:

3.1. PUPE FPGA Implementation

Instead of using an Alpha Data ADMXRC/FX10010/1G FPGA PMC module plugged onto the specially developed Compact PCI board of the pick-up processing engine, it was thought that it would be much better to simply integrate the ADMXRC's design directly onto the cPCI board. The same design would be used, it would be simply tracked onto the cPCI board itself. This would have a number of advantages:

- Cooling would be much better as the FPGA would face away from the carrier board and be in direct airflow.
- Allow the digital and analogue sections of the design to be placed more optimally to reduce noise.
- The PCB tracking would be better enabling cleaner and simpler interfaces between the board level components.

- One less PCI bridge chip would be needed reducing PCI bus latency.
- More of the FPGA's pins would be accessible allowing easier to integration of other interfaces to the FPGA such as Gigabit Ethernet ports.
- There would only be one Jtag interface for the whole board.

3.2. PUPE Gigabit links

The Virtex-4 FPGA has four on-board Gigabit Ethernet controllers. We thought that it would be good to connect two of these, via Gigabit PHY's to the cPCI's J3 connector to match the cPCI 2.16 switching backplane specification and provide another two Gigabit Ethernet interfaces via RJ45 ports on the front panel. This would allow the Gigabit Ethernet interfaces to be used in place of the cPCI bus for system communications in future developments. Using the Gigabit Ethernet ports would improve system communications bandwidth as the cPCI bus bottle neck is removed.

We envisage a future TMS that would have no cPCI module controllers. Each PUPE engine would run a simple, cut-down Linux system on one of the FPGA's power PC processors. The systems main controller would simply communicate directly with the PUPE's via a Gigabit Ethernet switch. This would provide a communications bandwidth of 1 Gigabit from each PUPE simultaneously if just one of the Gigabit interfaces were used. As the current projects time-scales are tight we would consider this a future development that could be performed if the PUPE had the Gigabit Ethernet interfaces implemented.

3.3. Timing Bus

Rather than using the cPCI's P3 connectors as a 8 channel timing bus, we could place a simple 16pin IDC connector in the front panel of each PUPE. This could then be simply connected using an 16 way IDC cable along the front of the units. This would provide accessibility from the front of the system for testing or special purposes.

3.4. Serial Timing Bus

As the timing buses signalling rates are low and they are re-synchronised to the 10MHz system clock on each PUPE it would be possible to serialise the timing signals along a single pair of cables rather than use 8 pairs. This would the number of timing signals to be increased easily and would simplify inter-board connections and hence improve reliability.