ADP-PUPE

Pickup Processing Engine

Hardware Manual

Revision 1.0

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PHOTO

1. Introduction

This document provides a hardware description of the ADP-PUPE board..

This board is based on two proprietary cards from Alpha Data - the ADM-XRC4FX card and the XRM-ADC-D2/125. These are combined to provide simultaneous 125 MHz sampling and capture of 9 analogue channels for processing and storage, either in on-board memory or on a remote host.

The board is implemented as a 6u CPCI board with a 64 bit interface and additional I/O via J3.

The target FPGA site for user applications can be fitted with either an XC4VFX100 or XC4VFX140 from Xilinx in a 1517 pin package to provide an extensive array of signal-processing , embedded processor and high-performance logic resources.

A separate Bridge / Control FPGA connects to the PCI bus and provides the Local Bus interface for the target FPGA. This bus is capable of operation at clock rates up to 80MHz. The Bridge FPGA also performs all of the board control functions, including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature in addition to providing high-performance PCI and DMA controllers

.Additional ports provide digital i/o for synchronisation, triggering and general communications use. This allows multiple boards to be operated in unison.

Four independent banks of 64Mx32 DDRII SDRAM (1GB total) connect to the target FPGA and are supported by Xilinx or third party IP.

Numerous clocking resources are provided for both sampling and user applications including user-clocks programmable between 31.25MHz and 625MHz, stable low-jitter 200MHz clock for precision IO delays, synchronisation to an external reference and low-jitter sampling clock distribution.

Serial flash memory is also connected to the target FPGA for user data.

Two 1G Ethernet ports are also provided.

This board is fully compatible with Alpha Data’s standard Software Development Kit (SDK) available for both Windows and Linux operating systems.

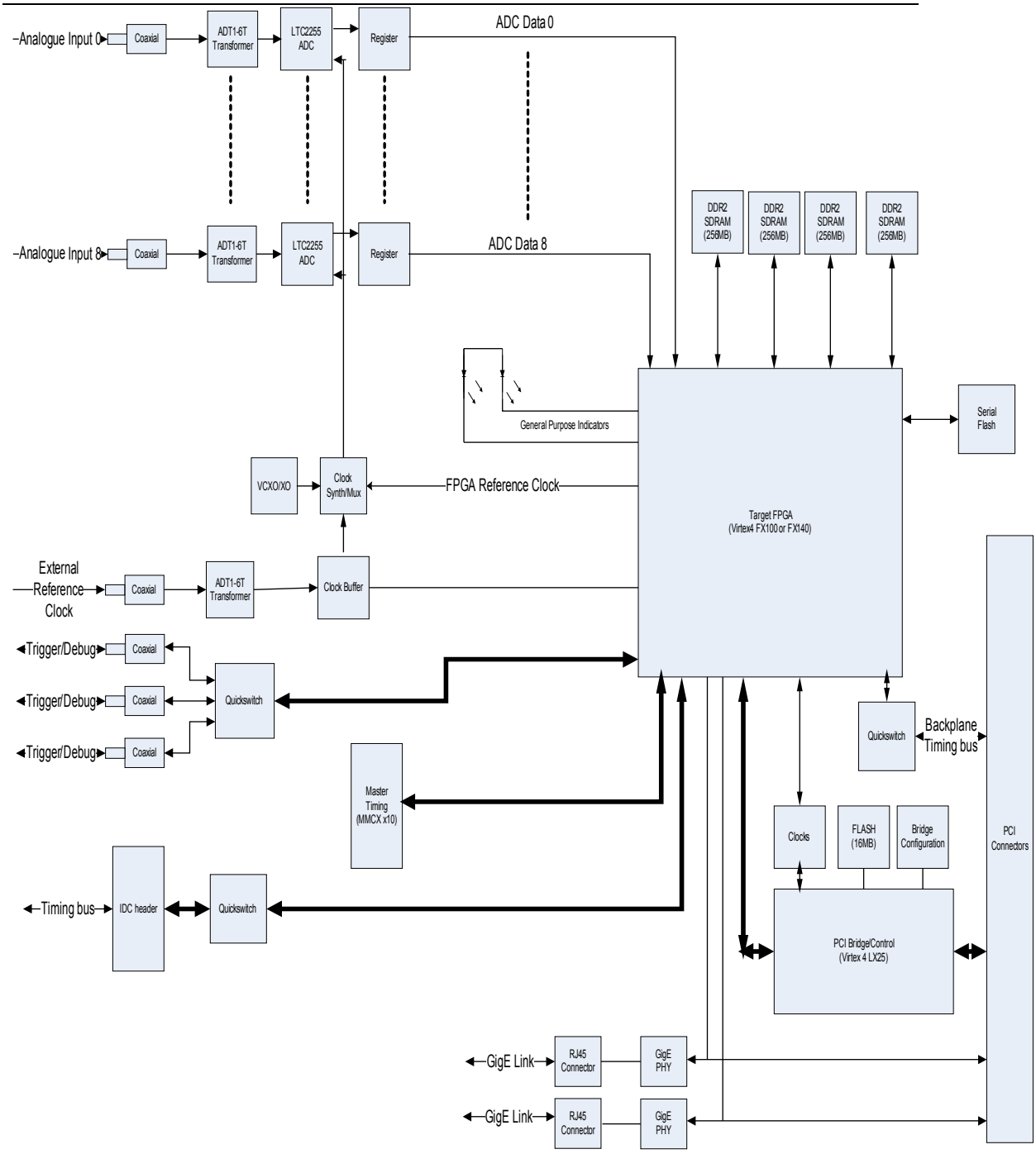


Figure 1 Block Diagram

1.1. Software Installation

Please refer to the installation CD. This contains the ADM-XRC SDK, driver. flash programming utilities, examples for host control and FPGA design and comprehensive help on application interfacing.

1.2. Related Documentation

ADM-XRC4FX User's manual

1.3. Example Code

Eaxample code, including 'C' application, example VHDL and UCF files, are available from the factory for this board.

2. CPCI Interface

The ADP-PUPE card is designed to meet PICMG CompactPCI® Core Specification 2.0 R3.0 and PICMG 2.16 R1.0 Packet Switching Specification.

The ADP-PUPE card is designed for RoHS-6 compliance.

2.1. Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

The ADP-PUPE card supports J1, J2 and J3 as per PICMG specifications. It does not implement hot-swap capability and is compliant only with 3.3V PCI signalling systems.

2.2. J1 Pin-out

J1 conforms to PICMG 2.0 R3.0.

2.3. J2 Pin-out

J2 conforms to PICMG 2.0 R3.0.

2.4. J3 Pin-out

J3 is provided to support PICMG 2.16 packet based switching using IEEE802.3-2000 1000BASE-T. It also serves as an alternate interface for the ADP-PUPE rack timing bus.

The pin assignment of J3 uses sparse population of signals. The timing bus signals, T1- to T8-, are located to avoid becoming aggressors to the differential signals of the two link ports. The link ports use spare BP(I/O) signals on rows 14 and 19 connected to ground for additional isolation.

19	GND	GND	GND	GND	GND	GND	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	GND	GND	GND	GND	GND	GND	GND

13	GND	NC	NC	NC	NC	NC	GND
12	GND						GND
11	(2)						(2)
10	(2)						(2)
9	(2)						(2)
8	GND						GND
7	GND						GND
6	GND	T1+	T2+		T3+	T4+	GND
5	GND						GND
4	GND	T5+	T6+		T7+	T8+	GND
3	GND						GND
2	GND	T9+	T10+				GND
1	GND	(1,16)	(1,16)	(1,16)	(1,16)	(1,16)	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 1 CPCI J3 Pin Assignments

Notes.

1,16 Refer to PICMG 2.16 R1.0.

3. Local Bus Resources

3.1. Local bus description

The ADP-PUPE implements a multi-master local bus between the bridge and the target FPGA using a 32- or 64-bit multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

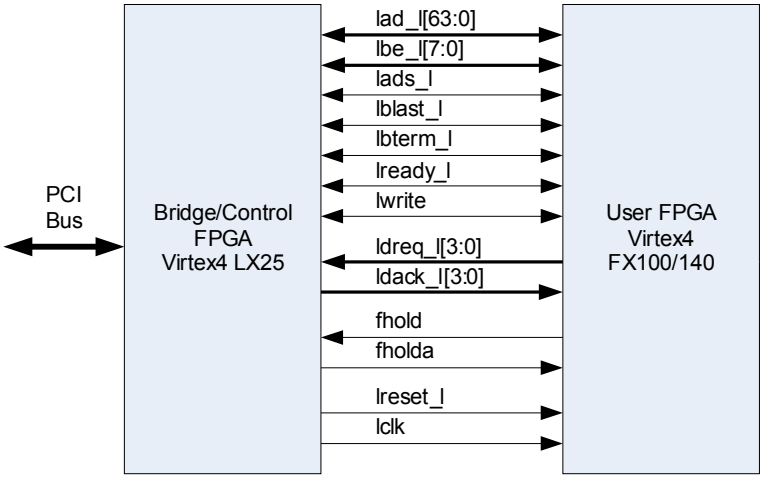


Figure 2 Local Bus Interface

Signal	Type	Purpose
lad[0:63]	bidir	Address and data bus.
lbe_l[0:7]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[0:3]	unidir	DMA request from target to bridge
ldack_l[0:3]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 2 Local Bus Interface Signal List

3.2. Health Monitoring

The ADP-PUPE has the ability to monitor temperature and voltage of key parts of the board to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the board control logic connected using I^2C.

The Control Logic scans the LM87 when instructed by host software and stores all current voltage and temperature measurements in a blockram. This allows the values to be read without the need to communicate directly with the monitor.

Power supplies and temperatures can be monitored , as shown in Table 3 Voltage and Temperature Monitors'.

Monitor	Purpose
1.2V	Bridge FPGA Core Supply
1.5V	Supply for MGT linear regulators
1.8V	Memories, User FPGA Memory I/O, Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front, Rear I/O
3.3V	Board Input Supply
5.0V	Board Input Supply
PN4_VCCIO	Either 2.5V or 3.3V Rear I/O (Pn4) Voltage
XRM_VCCIO	Either 2.5V or 3.3V Front Panel I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 3 Voltage and Temperature Monitors

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

```
*** SysMon ***

FPGA    Space Base Adr = 00900000
Control Space Base Adr = 00d00000


+1V2 Reading = 1.21 V
+1V5 Reading = 1.51 V
+1V8 Reading = 1.81 V
+2V5 Reading = 2.51 V
+3V3 Reading = 3.32 V
+5V  Reading = 5.04 V
Pn4  Reading = 3.31 V
FPIO Reading = 3.34 V

SysMon Int Temp =   33 deg. C
User FPGA Temp  =   26 deg. C
```

3.3. Configuration

The ADP-PUPE allows configuration of the target FPGA from the host at high speed using SelectMAP. The FPGA may also be configured from flash (programmable from the host) or by JTAG via header J7.

Download from the host is the fastest way to configure the User FPGA with 8-bit SelectMAP mode enabled. This permits a theoretical configuration speed of up to 40MB/s.

The ADP-PUPE can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the clocks and I/O voltages as appropriate.

NOTE: Boards supplied with Engineering Silicon (ES) and Production Stepping 0 will already have a bitstream in the flash. This will be loaded on power up of the card. This default bitstream maintains the requirements for the static operating behaviour of the RocketIO transceivers. See Xilinx Answer Record #22471 for further details.

4. Memory

The ADP-PUPE is fitted with two separate Flash memories; one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.1.1. Board Control Flash

An Intel PC28F256P30 flash memory is used for storing a configuration bitstream for the User FPGA. Once the Bridge / Control FPGA is configured, it checks for a valid bitstream in flash and, if present, automatically loads it into the User FPGA. This process can be inhibited by setting a jumper on the JTAG connector. See the description of the “FBS” signal in Section 9.1 for further information.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus.

Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

4.1.2. User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

4.2. DDRII SDRAM

The ADP-PUPE has 4 independent banks of DDRII SDRAM. Each bank consists of two memory devices in parallel to provide a 32 bit data path. 1Gb Micron MT47H64M16 devices are fitted as standard to provide 256MB per bank. The board will support higher capacity devices when they become available.

The ADP-PUPE has been designed for compatibility with Xilinx memory interface cores. Details of the signalling standards, bank numbers etc. are given in the tables below:

Name	Direction	I/O Standard	Bank
DDR1_ad[15:0], DDR1_ba[2:0], DDR1_rasn, DDR1_casn, DDR1_wen, DDR1_csn, DDR1_cke, DDR1_odt	Output	SSTL18_I_DCI	2, 11
DDR1_ck0, DDR1_ckn0	Output	DIFF_SSTL18_II	11
DDR1_dq[15:0]	BiDir	SSTL18_II	11
DDR1_dm[1:0]	Output	SSTL18_II_DCI	11
DDR1_dqs[1:0], DDR1_dqsn[1:0]	BiDir	DIFF_SSTL18_II	11
DDR1_ck1, DDR1_ckn1	Output	DIFF_SSTL18_II	11
DDR1_dq[31:16]	BiDir	SSTL18_II	11
DDR1_dm[3:2]	Output	SSTL18_II_DCI	11
DDR1_dqs[3:2], DDR1_dqsn[3:2]	BiDir	DIFF_SSTL18_II	11

Table 4 DDR Memory Bank1 Configuration

Name	Direction	I/O Standard	Bank
DDR2_ad[15:0], DDR2_ba[2:0], DDR2_rasn, DDR2_casn, DDR2_wen, DDR2_csn, DDR2_cke, DDR2_odt	Output	SSTL18_I_DCI	2, 7
DDR2_ck0, DDR2_ckn0	Output	DIFF_SSTL18_II	7
DDR2_dq[15:0]	BiDir	SSTL18_II	7
DDR2_dm[1:0]	Output	SSTL18_II_DCI	7
DDR2_dqs[1:0], DDR2_dqsn[1:0]	BiDir	DIFF_SSTL18_II	7
DDR2_ck1, DDR2_ckn1	Output	DIFF_SSTL18_II	7
DDR2_dq[31:16]	BiDir	SSTL18_II	7
DDR2_dm[3:2]	Output	SSTL18_II_DCI	7
DDR2_dqs[3:2], DDR2_dqsn[3:2]	BiDir	DIFF_SSTL18_II	7

Table 5 DDR Memory Bank2 Configuration

Name	Direction	I/O Standard	Bank
DDR3_ad[15:0], DDR3_ba[2:0], DDR3_rasn, DDR3_casn, DDR3_wen, DDR3_csn, DDR3_cke, DDR3_odt	Output	SSTL18_I_DCI	12
DDR3_ck0, DDR3_ckn0	Output	DIFF_SSTL18_II	14
DDR3_dq[15:0]	BiDir	SSTL18_II	14
DDR3_dm[1:0]	Output	SSTL18_II_DCI	14
DDR3_dqs[1:0], DDR3_dqsn[1:0]	BiDir	DIFF_SSTL18_II	14
DDR3_ck1, DDR3_ckn1	Output	DIFF_SSTL18_II	14
DDR3_dq[31:16]	BiDir	SSTL18_II	14
DDR3_dm[3:2]	Output	SSTL18_II_DCI	14
DDR3_dqs[3:2], DDR3_dqsn[3:2]	BiDir	DIFF_SSTL18_II	14

Table 6 DDR Memory Bank3 Configuration

Name	Direction	I/O Standard	Bank
DDR4_ad[15:0], DDR4_ba[2:0], DDR4_rasn, DDR4_casn, DDR4_wen, DDR4_csn, DDR4_cke, DDR4_odt	Output	SSTL18_I_DCI	12
DDR4_ck0, DDR4_ckn0	Output	DIFF_SSTL18_II	8
DDR4_dq[15:0]	BiDir	SSTL18_II	8
DDR4_dm[1:0]	Output	SSTL18_II_DCI	8
DDR4_dqs[1:0], DDR4_dqsn[1:0]	BiDir	DIFF_SSTL18_II	8
DDR4_ck1, DDR4_ckn1	Output	DIFF_SSTL18_II	8
DDR4_dq[31:16]	BiDir	SSTL18_II	8
DDR4_dm[3:2]	Output	SSTL18_II_DCI	8
DDR4_dqs[3:2], DDR4_dqsn[3:2]	BiDir	DIFF_SSTL18_II	8

Table 7 DDR Memory Bank4 Configuration

5. Clocking

The ADP-PUPE has two clock distribution schemes, one for clocking the FPGA logic and one for the clocking the sampling circuitry, as illustrated below:

5.1. Logic Clocks

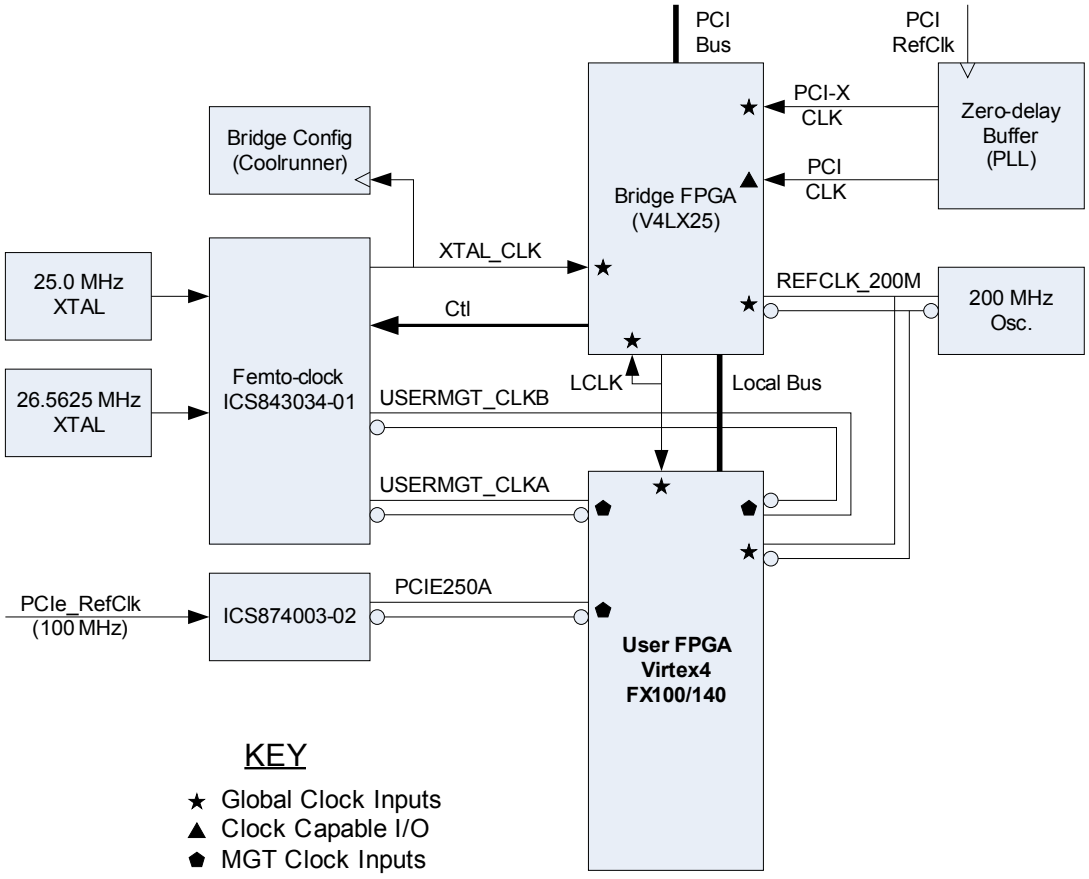


Figure 3 FPGA Logic Clock Distribution

5.1.1. LCLK

The Local Bus can be used at up to 80 MHz and all timing is synchronised to LCLK between the Bridge and User FPGAs. LCLK is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz.

The LCLK frequency is set by writing to the board control logic. (See SDK for details and example application).

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

5.1.2. REFCLK

In order to make use of the IDELAY features of Virtex™-4, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADP-PUPE is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

5.1.3. PCIe Reference Clock

A 100MHz PCIe reference clock input from the Primary XMC connector (Pn15) is converted to 250MHz by an ICS874003-02. The 250MHz clock is then connected to one of the dedicated MGT clock inputs on the user FPGA. (See Figure 3 for details of the MGT clock connections.)

5.1.4. User Clocks

A programmable, low-jitter clock source is provided by an ICS843034-01 “FemtoClocks” frequency synthesiser. The synthesiser has two source crystals – one at 26.5625MHz and another at 25.0MHz . The synthesiser also has two clock outputs.

”USERMGT_CLKA” is connected to the MGT clock input on one side of the user FPGA.

”USERMGT_CLKB” is connected to the MGT clock input on the other side of the user FPGA.

These low-jitter (around 1ps rms) programmable clock sources, originally used to generate clocks for the Multi-Gigabit Transceivers in the ADM-XRC-4, can be used within the fabric of the FPGA to provide a flexible clock source. e.g. as a sampling clock when an external source is not available or where it is not necessary to synchronise to an external system.

The selection of the clock frequency to be generated by the Femtoclock is controlled by the PCI bridge in the FPGA processor and is fully supported by the ADP-PUPE driver.

Note: The Virtex 4FX MGT outputs and inputs are not accessible on the ADP-PUPE.

5.1.5. PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be removed to provide full PCI 33MHz compatibility.

5.2. Sample Clocks

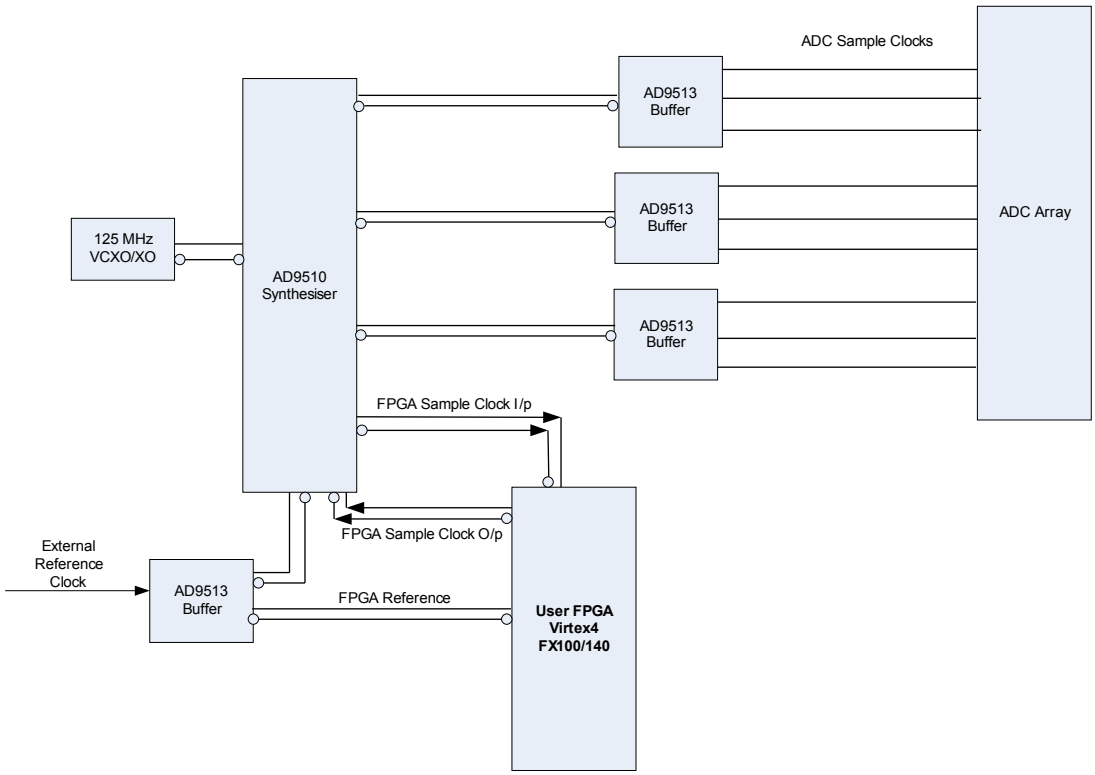


Figure 4 Sampling Clock Distribution

5.3. Clock Synthesis

All 9 analogue inputs on the ADP-PUPE are sampled synchronously using a common sampling clock. Particular care is applied to clock distribution to minimise jitter and skew to thus ensure synchronisation of all channels. Clock source selection and control over synthesis of the sampling clock is performed by the FPGA processor.

5.3.1. Sample Clock Generation

The synthesis of the sampling clock is performed by an Analog Devices AD9510 which normally uses a VCXO to provide a stable low-jitter clock running at 125MHz. A fixed crystal oscillator can be substituted for stand-alone operation.

The sample clock signal is fed to four output stages in the AD9510 , three of which are routed to AD9513 1:3 clock buffers which in turn drive the clock inputs of the nine A to D converters. The remaining AD9513 output is fed as a differential pair to the FPGA as a sampling clock reference to ensure synchronous operation of the FPGA and the ADCs .

The FPGA can also be used to provide a sample clock independent of any external reference for stand alone operation/test functions.

Note that each group of 3 ADCs can be also be clocked at different rates by specifying different divider ratios within the AD9510.

5.3.2. Synthesiser Control

Programming of the 9510 is accomplished by a 4-wire interface controlled via the FPGA. This sets the PLL and output divider ratios and the selection of clock source. Control of the synthesiser also allows sampling clock frequencies other than 125MHz or reference clock frequencies other than the standard 10 MHz to be utilised. Customisation of the PLL filter to suit such configurations can be implemented.

5.3.3. Synthesis Reference Clock

The ADP-PUPE can be synchronised to an external 10MHz reference clock in order to generate the 125MHz sampling clock for the converters. The board also has a number of options to allow it to operate without an external reference, either by using the 125 MHz oscillator or an FPGA-generated clock.

The external reference is also fed to the FPGA for synchronisation, general and/or test use.

The reference clock input can accept TTL level inputs and provides 50 Ohm routing and termination.

6. Ethernet

Two 10M/100M/1G Ethernet ports are provided. Each port uses an RJ-45 connector with integrated magnetics coupled to a National Semiconductor DP83865 'MacPhyter' to implement the physical layer whilst the MAC is provided in the Virtex 4FX as a hard macro. Users must implement their own TCP/IP stack and any required control logic or CPU in order to use these ports.

Features such as auto-negotiation, link speed, etc. can be configured via the serial management interface pins connected to the FPGA.

Each PHY has a dedicated 25 MHz clock oscillator and can be routed to the backplane via J3 in compliance with PICMG 2.16 instead of the front panel.

The PHYs are controlled using an RGMII interface; note that this requires the implementation of a skew between receive data and clock of 1.0 ns to 2.6 ns. In the ADP-PUPE this is implemented by looping back the requisite clock signal via a pair of FPGA pins.

6.1. Configuration

Th Ethernet connections from the two PHYs can be routed via the front-panel RJ45 connectors (default) or optionally via J3 . The routeing for each PHY can be set independently but each PHY must be connected to only one interface (either J3 or front panel) by fitting OR resistors as indicated in the table below.

Channel	RJ45	J3
PHY 0	R565,R573,R577,R580,R591,R596,R603,R607	**R564,R572,R576,R579,R590,R595,R602,R606**
PHY1	**R648,R653,R658,R662,R669,R673,R678,R681**	**R647,R652,R657,R661,R668,R672,R677,R680**

7. Analogue

There are 9 analogue inputs on the ADP-PUPE card all of which sample synchronously using a common sampling clock.

7.1. Input Stage

Each analogue input is ac-coupled via a 1:1 transformer and 6 dB pad., providing an input impedance of 50R. The input pad and transformer type can be factory customised to suit specific applications. The input connector and its associated ground are isolated from the board ground.

7.2. ADC Stage

Each converter Is powered by a dedicated 3V0 regulator. The internal ADC full scale scaling is set to +/-1 V by means of factory-configurable jumper settings. When coupled with the 6dB pad this means that the full scale limits of the ADC are equivalent to +/- 2 V at the input connector.

Data skews between ADC channels is minimised by trace length balancing hence data from all channels can be acquired using the single copy of the sample clock connected to the FPGA. Any further deskewing can be implemented in the FPGA if required, although this is not normally the case.

The data captured from each channel is buffered and fed to the FPGA for storage or processing prior to transfer to the host system. All data output from the ADC is in 2's complement format.

The over range bit for each channel is also routed back to the FPGA in the same way as the data to provide an indication of an overload situation.

7.3. ADC Control

Each converter has a MODE pin and a SENSE pin which can be configured by jumpers to set ADC scaling, output format and internal duty cycle correction. These functions are factory configurable only and not under control of the FPGA.

In addition, the FPGA supplies 1 control line to all converters (tied to the OE and SHDN pins) to allow for global on/off control of the ADCs

8. Digital I/O

8.1. Debug I/O

There are 3 FPGA pins dedicated to input or output of debug signals directly from the FPGA. directly to front-panel connectors.

8.2. I/O Front Panel

A separate front panel suitable for use with the ADP-PUPE is available This provides conforms to IEEE1101.10 (EMC Panels).

The timing bus is a set of signals sourced from other CERN equipment that is used to synchronise activities in the ADP-PUPE card with all other ADP-PUPE cards in the system. The timing bus is received by a master ADP-PUPE card via a timing input panel and distributed to 3 or 4 slave cards in the same rack using either front panel or backplane interconnect.

The timing bus can accommodate up to 10 signals. The firmware loaded into the FPGA determines how these timing signals are interpreted.

All of the timing signals can be synchronised to the 125MHz or the 10MHz refernce clock (default) by the master ADP-PUPE and output onto the timing bus for all slaves to read. The mastercan also read back from its own pins in order to ensure that all boards see the same timeing of the various signals.

8.3. Timing Bus Operation

The timing system consists of three parts; master timing input, front panel timing bus and backplane timing bus.

The master timing input uses 10 pins on the FPGA to receive system wide timing information via the ADP-PUPE I/O Panel.

The front panel timing bus is a bidirectional interface shared between ADP-PUPE cards using 10 FPGA pins on a 20 pin header to output data from a master card and input data on a slave card.

The backplane timing bus is also a bidirectional interface shared between ADP-PUPE cards and uses 10 FPGA pins connected to J3 of CPCI interface.

8.4. Master Mode Inputs

The master mode timing inputs are received via PCB mounted vertically orientated MCX connectors from the ADP-PUPE I/O panel.

The inputs are protected using Quickswitches to allow up to 5V signalling at the connector whilst limiting the actual FPGA pin voltage to 2.5V - see 9.2.

All inputs are routed and terminated with 50Ω impedance.

8.5. Master/Slave Timing Interface

The master/slave timing interface permits a ADP-PUPE card to send or receive timing signals on a front panel connector to or from adjacent cards in the rack using a ribbon cable based bus. The signals are connected directly to the FPGA through a Quickswitch for protection.

All of the signals on the bus are single ended and terminated in the characteristic impedance of the cable.

The last slave card in the rack implements the termination although all cards have the option to do so - see 9.2.

All of the timing signals are 3.3V LVTTL compatible.

8.6. Optional J3 Master/Slave Timing Interface

A similar set of timing signals are available for output on J3 and may be used in addition to or instead of those on the front panel. See also 9.2

8.7. Header Bus

The connector used on the front panel is a Molex part, number 87833-2019 which mates with the Molex 87568 series IDC receptacle.

The pin-out of the connector is shown below.

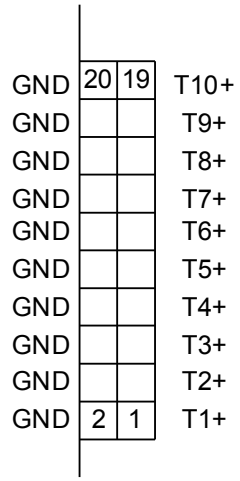


Figure 5 Front Panel Timing Bus

8.8. ADP-PUPE I/O Panel Assembly

The ADP-PUPE I/O Panel is compliant with IEEE1101.10 and serves the purpose of interfacing externally provided timing signals to a master ADP-PUPE card. The master ADP-PUPE card then distributes the timing signals to up to 4 other ADP-PUPEs within the same cPCI rack via the header bus.

The ADP-PUPE I/O panel allow connections to be made easily rather than directly onto the ADP-PUPE card itself which may cause mechanical stress.

The function of each of the timing signals on the panel is determined by the functionality implemented by the FPGA processor based on system requirements.

The layout of the 6U panel is shown below.

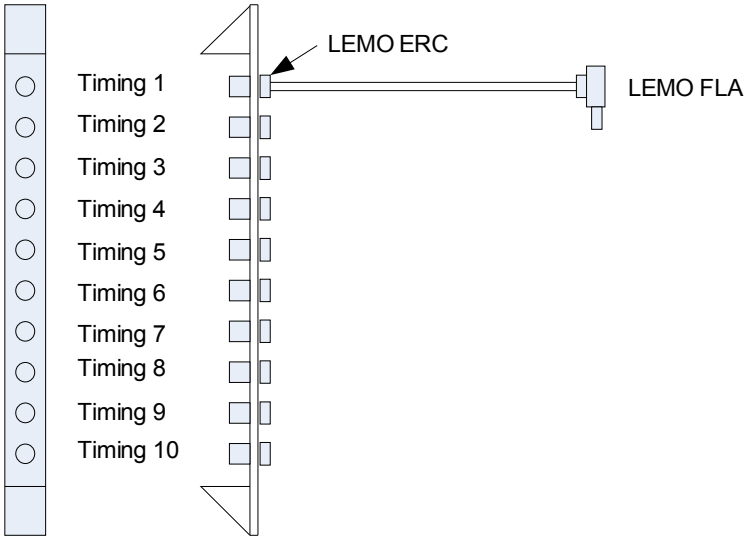


Figure 6 ADP-PUPE I/O Panel Outline

This is an option.

9. Miscellaneous

9.1. JTAG

A JTAG header is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that four devices will be detected when the SCAN chain is initialised.

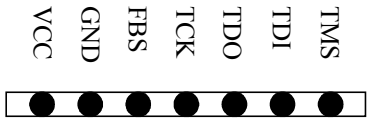


Figure 7 JTAG Header

The VCC supply provided on J5 to the JTAG cable is +2.5V and is protected by a poly fuse with a rating of 350mA.

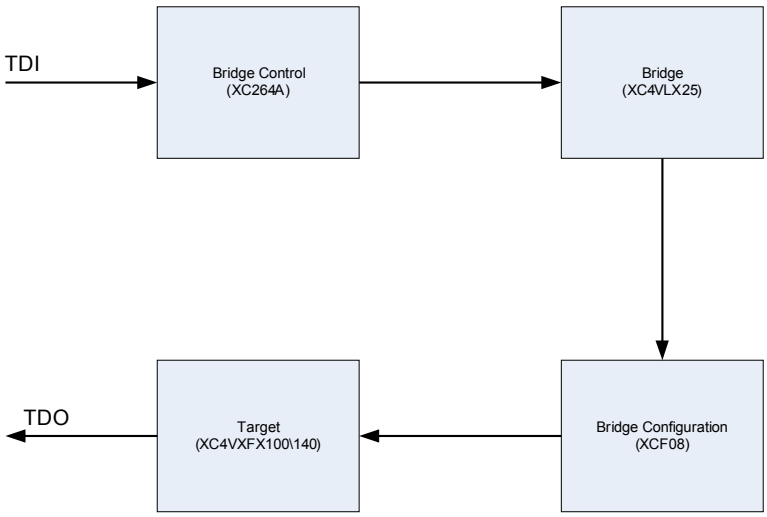


Figure 8 ADP-PUPE JTAG Loop

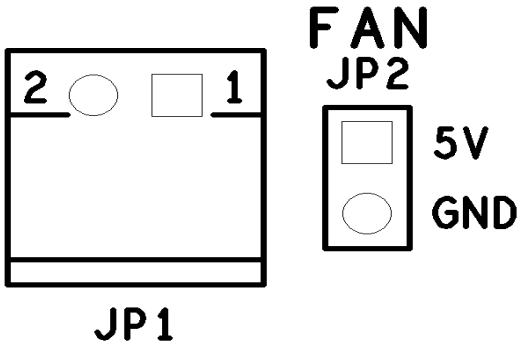
9.1.1. FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

9.2. Jumper Functions

JP1 - +5V supply for heatsink/fan. Pin 1 = +5V

JP2 - +5V supply for heatsink/fan. Pin 1 = +5V



JP3 - J3 timing bus enabled when shorting link fitted (see 8.6)

JP4 - Master timing bus inputs enabled when shorting link fitted (see 8.4)

JP5 - Terminations enabled when shorting link fitted (see 8.5)

JP6 - Header timing bus inputs enabled when shorting link fitted (see 8.7)

Important note - JP1 and JP2 provide +5V/0V for fan connections only. Shorting headers must not be fitted in the these positions.

9.3. Test points

A total of 6 general-purpose test pads are available for bench debugging of signals in real-time via a scope or similar.

9.4. LEDs

Two bi-colour LEDs are provided for use as status indicators for debug and general signalling purposes. These can be driven directly from the FPGA

9.5. I/O Bank Voltages

Bank	Voltage	Description
0	2.5V	Configuration I/F
1, 6	1.8V	Local Bus
2, 7, 8, 11, 12, 14	1.8V	SelectMAP I/F, DDRII DRAM I/O
3, 4	3.3V	Clocks, Serial Flash, DebugI/O
5, 9, 13	2.5V	ADC Interface
10	2.5V	Phy Interface, Timing Bus

Table 8 User FPGA I/O Bank Voltages

10. Performance Specification

.Power Consumption

+5V 1A typical

+3V3 2A typical

Typical figures when running the test application.

10.1. Analogue Inputs

Converter	Linear Technology LTC2255
Maximum Sample Rate	125Ms/s
Input level	full scale +/- 2V[1] (+16dBm), protected to +/- 4V
Input impedance	50Ω, transformer coupled
Input bandwidth	-3dB from 30kHz to 125MHz
Input filter	none
Coupling	transformer
SNR	>70dB
SFDR	>70dB
ENOBS	>10.5
Input connector	SMA / LEMO00

10.2. Reference Clock Input

Input level	nominal +/- 1V, protected to +/- 4V
Input impedance	50Ω, transformer coupled
External frequency	10MHz nominal
Input connector	SMA/LEMO00

10.3. Sampling Clock

Sampling frequency	125 MHz max, synchronised to external reference or internally generated
Distribution Jitter	< 5ps RMS

[1] with standard 6 dB input pad - factory customisation available

10.4. General Purpose Digital I/O

Type: Bidirectional

Coupling : DC

Output : Buffered LVCMOS

Output Voltage : 3V3 (default) or 5V (factory selectable)

Output Termination: 4k7 to ground

Input : Buffered LVCMOS, 5V tolerant

Input Voltage : 3V3 (default) or 5V (factory selectable)

Input Termination: 50R

Connector SMA/LEMO00

10.5. Master Bus Digital Inputs

Type: Input[2], 5V tolerant

Coupling : DC

Input Termination: 50R

Connector : MCX

10.6. Header Bus Digital I/O

Type: Bidirectional

Coupling : DC

Output : LVCMOS

Output Voltage : 2V5

Input : LVCMOS, 3V3 tolerant

Input Voltage : 2v5

Connector Molex 87833-2019

Note: this bus is typically used for synchronisation of multiple ADP-PUPEs via a ribbon cable assembly. Any ADP-PUPE can be configured to provide termination for this bus, but this should be enabled on only one card on the bus.

10.7. Backplane Bus Digital I/O

Type: Bidirectional

Coupling : DC

[2] Factory configurable as 5v tolerant inputs, 2V5 outputs

Output : LVCMOS

Output Voltage : 2V5

Input : LVCMOS,

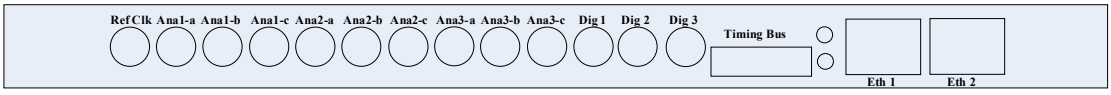
Input Voltage : 2v5

Connector CPCI J3

Use of this bus requires a suitable rear transition module.

10.8. Front Panel Diagram

When fitted in a 6U high rack, the Ethernet connections are at the bottom of the board.



11. Revision History

Date	Revision	Nature of Change
03-10-2007	1.0	Created